



- Alumina Cofired Ceramic Flip Chip Package -

General Design Guide



Contents

1. General

1-1 Out Line

1-2 Plating condition

1-3 Applicable Layer Thickness

1-4 Properties

2. Dimensional Specifications

2-1 Out Line

2-2 Flip Chip Area

2-3 Coplanarity

3. Internal Design Rule

3-1 Flip Chip Area

3-2 Outside Flip Chip Area

4. Design Rule Road Map



1. General

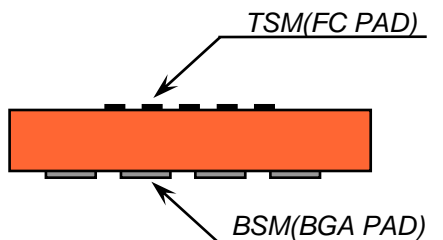
1-1 Out Line

UNIT:mm

Item	Standard	Special
Size	≤ 50 sq.	≤ 94 x 100
Layer Thickness	0.127 0.152 0.203 0.254 0.381 0.508 0.635	0.040 (2mil tape) 0.102
Substrate Thickness	≤ 3.30	≤ 5.08
Layer Count (reference)	20 Max.	30 Max.

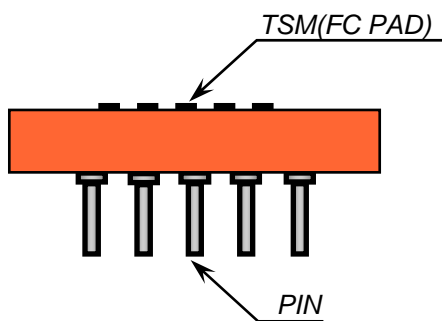
1-2 Plating Condition

1-2-1 Flip Chip BGA



TSM	BSM
Electroless Ni (3.2 μ m Min.) +Electroless Au(0.03~0.10 μ m)	Electroless Ni (3.2 μ m Min.) +Electroless Au(0.03~0.10 μ m)

1-2-2 Flip Chip PGA



TSM	PIN (BSM)
Electroless Ni (3.2 μ m Min.) +Electroless Au(0.03~0.10 μ m)	Electrolytic Ni (2.0 μ m Min.) +Electrolytic Au(1.27 μ m Min.) (with Pin Through Plating)



1-3 Applicable Layer Thickness

(A) Ability of Via Filling

Via Dia (μm)	THK	Special Sheet		STD. Sheet						
		0.040 mm (2 mil)	0.102mm (4 mil)	0.127mm (5 mil)	0.152mm (6 mil)	0.203mm (8 mil)	0.254mm (10 mil)	0.381mm (15 mil)	0.508mm (20 mil)	0.635mm (25 mil)
70 μm		✓	✓	✓	✓					
95, 100 μm		✓	✓	✓	✓	✓	✓	Need divide into some thinner sheets		
130, 150 μm		✓	✓	✓	✓	✓	✓	✓		
200 μm		✓	✓	✓	✓	✓	✓	✓	✓	✓

- Note 1. NTK recommends to use 6 mil sheet for a top (F/C pad) layer.
2. Use of special sheet thickness should be discussed with the NTK engineering.

(B) Ability of Via Punching

Via Pitch	THK	Special Sheet		STD Sheet			
		0.040 mm (2 mil)	0.102mm (4 mil)	0.127mm (5 mil)	0.152mm (6 mil)	0.203mm (8 mil)	0.254mm (10 mil)
250 μm (100 μm dia.)							
225 μm (95 μm dia.)		Gang Punching					
200 μm (95 μm dia.)							
180 μm (70/95 μm dia.)				Block (Semi-hard) Punching			

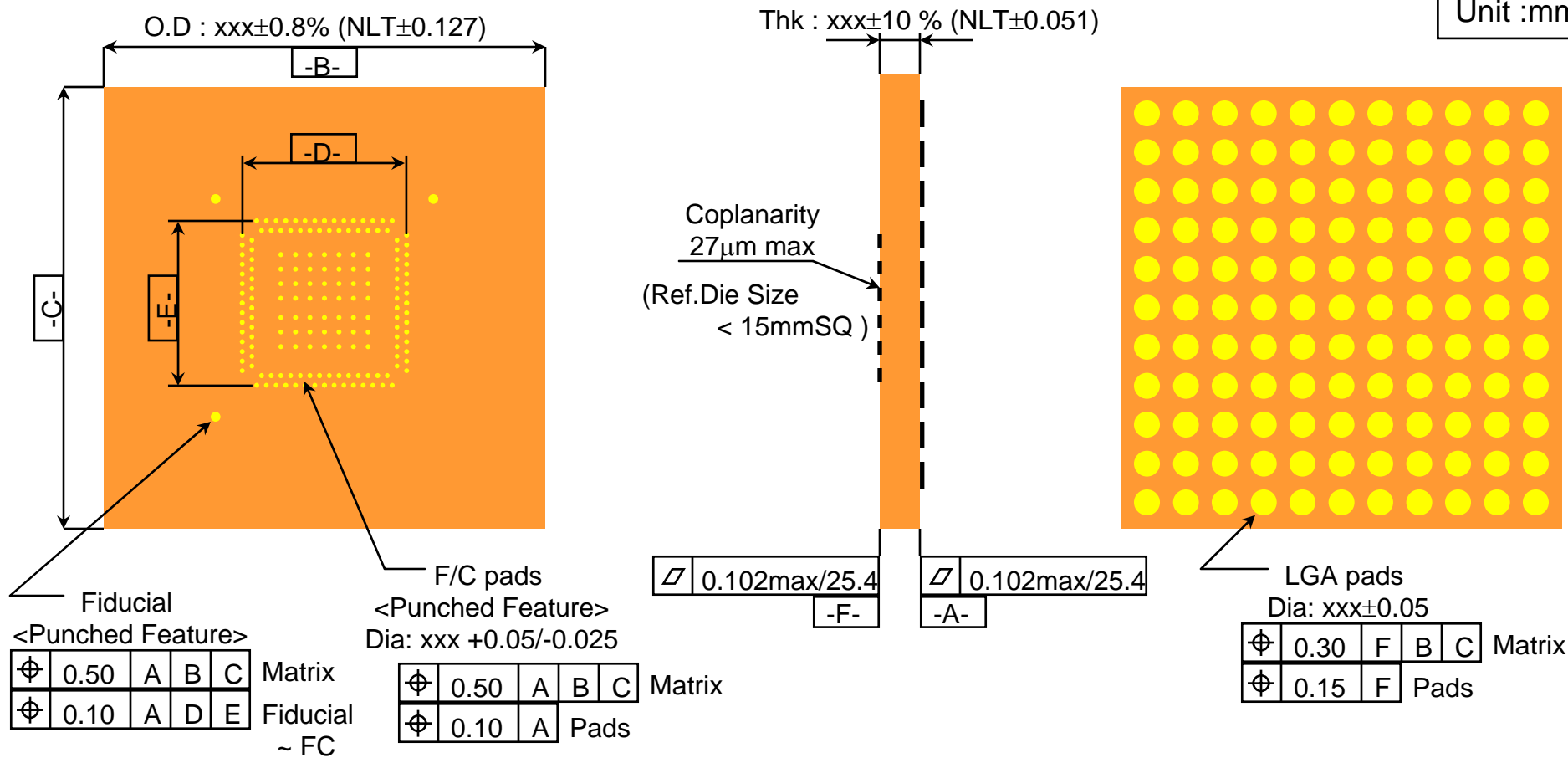


1-4 Properties

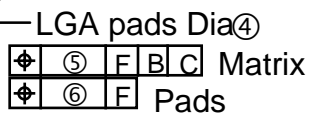
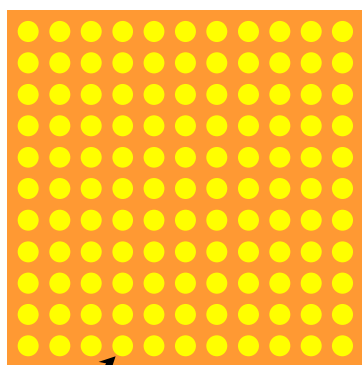
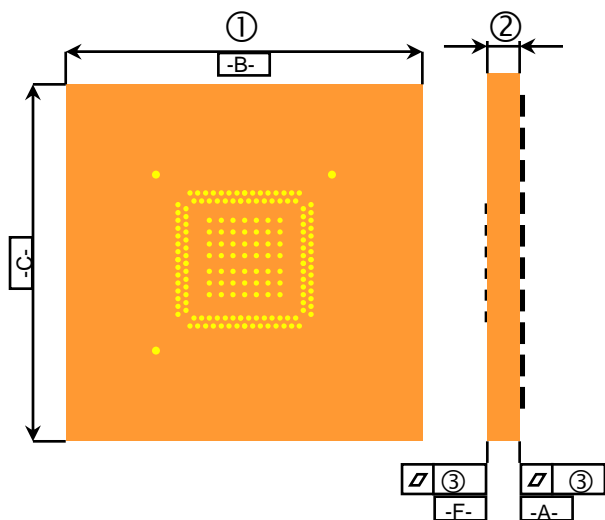
Item	Unit	Value
<i>TCE (RT~800deg.C)</i>	<i>[ppm/deg.C]</i>	<i>7.6</i>
<i>(RT~400deg.C)</i>	<i>[ppm/deg.C]</i>	<i>6.8</i>
<i>Thermal conductivity</i>	<i>[W/m deg.C]</i>	<i>17</i>
<i>Dielectric constant</i>		<i>9.8(@1MHz)</i> <i>9.0(@10GHz)</i>
<i>Dielectric loss</i>		<i>0.0004(@1MHz)</i> <i>0.0010(@10GHz)</i>
<i>Volume Resistivity</i>	<i>[ohm.m]</i>	<i>>10¹²</i>
<i>Young Modulus</i>	<i>[GPa]</i>	<i>280</i>
<i>Bending Strength</i>	<i>[MPa]</i>	<i>350</i>
<i>Conductor Resistance</i> <i>(100μm w trace : Mo)</i>	<i>[mohm/sq.]</i>	<i>8</i>

2. Dimensional Specifications

Unit :mm



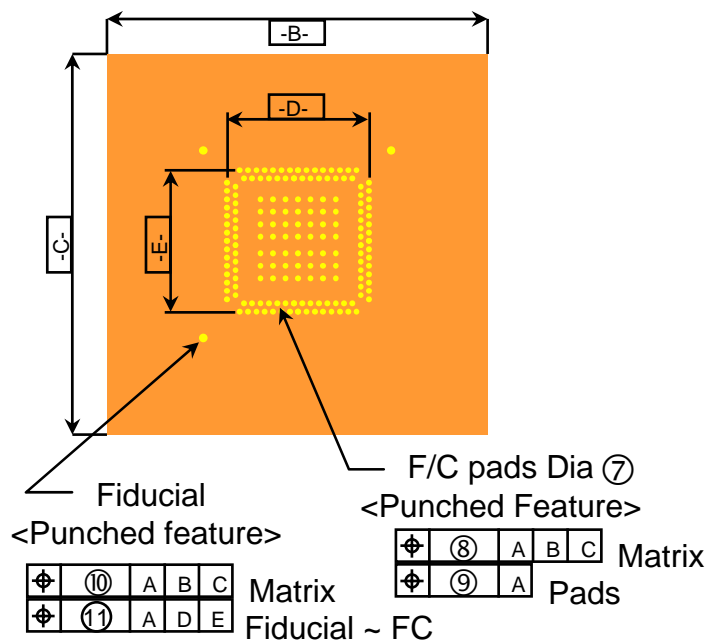
2-1 Out Line



Unit : mm

	Std.	Special
① O.D	+/- 0.8% NLT 0.127	+/- 0.5% NLT 0.10
② Thk.	+/- 10% NLT 0.05	+/- 5% NLT 0.04
③ Flatness	0.102 Max /25.4	0.051 Max /25.4
④ LGA Pad Dia.	+/- 0.05	
⑤ Matrix True Position (PKG center ~ LGA center)	0.30 (+/- 0.15)	0.20 (+/- 0.10)
⑥ Pad ~ Pad True Position (Total Pitch)	0.15 (Total P : +/-0.15)	0.10 (Total P : +/-0.10)

2-2 Flip Chip Area



Unit : mm

	Std.	Special
⑦ F/C Pad Dia.	+ 0.051 - 0.025	+/- 0.025
⑧ Matrix True Position (PKG center ~ F/C center)	0.50 (+/- 0.25)	0.25 (+/- 0.127)
⑨ Pad ~ Pad True Position (Total Pitch)	0.10 (Total P : +/-0.10)	+/- 0.3% NLT 0.04
⑩ Matrix True Position (PKG center ~ Fiducial center)	0.50 (+/- 0.25)	0.25 (+/- 0.127)
⑪ Fiducial ~ FC True Position (F/C Matrix center ~ Fiducial)	0.10 (+/- 0.05)	

2-3 Coplanarity < Least Square Method >

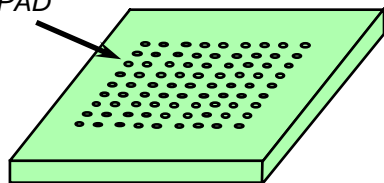
Standard Coplanarity Specification for reference

CHIP SIZE	≤ 10mmSQ.	≤ 15mmSQ.	≤ 20mmSQ.
Standard Coplanarity Specification	20μm MAX.	27μm MAX.	38μm MAX.

<DEFINITION OF COPLANARITY>

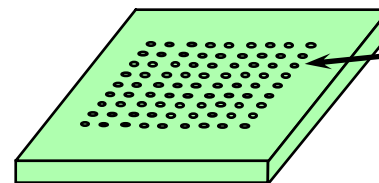
Step 1 Making Imaginary Plane

MEASUREMENT PAD
(25 PADS)



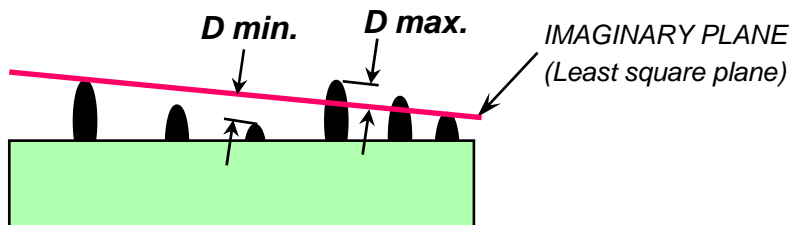
* Make the imaginary plane by using 25 F/C pads position (x,y,z).
< Imaginary plane is defined by least square plane method using 25 points. >

Step 2 Measurement of Coplanarity



MEASUREMENT PAD
(25 PADS)

* Calculate the distance between imaginary plane (Least square plane) and 25 F/C pads (D1 ~ D25).

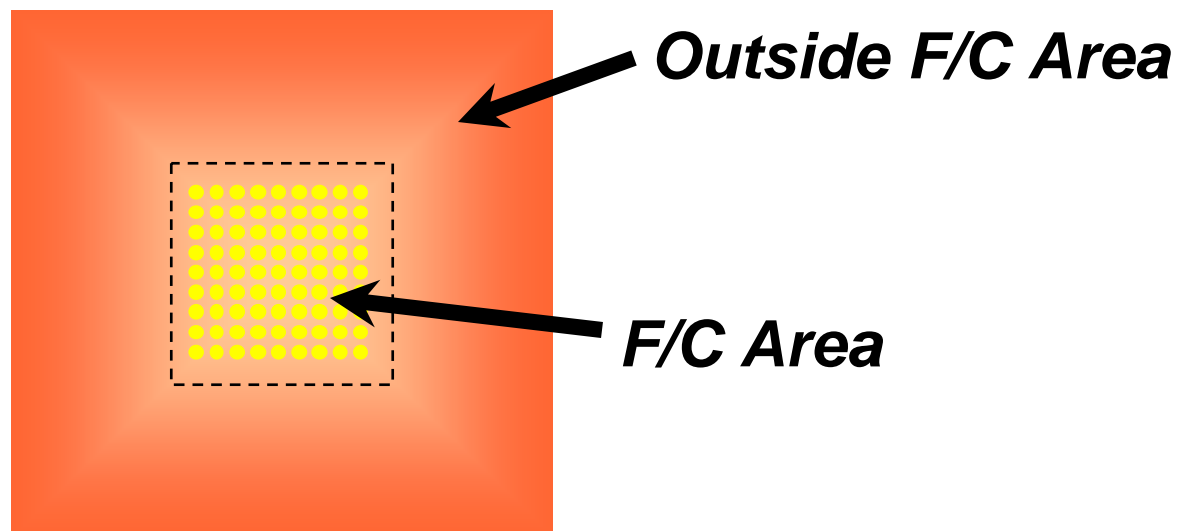


$$\text{COPLANARITY} = D_{\text{max.}} + D_{\text{min.}}$$

3. Internal Design Rule

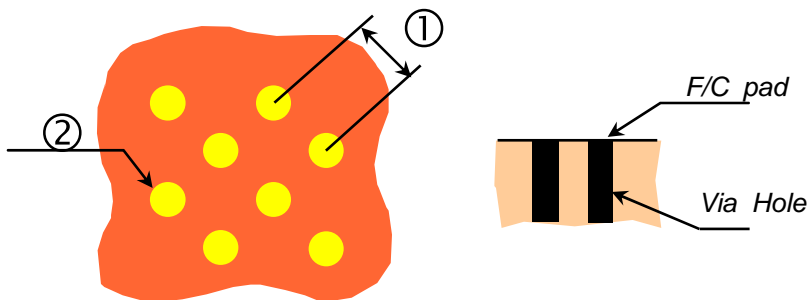
Design Rules are separated into “Fine Rule” Area & “Regular Rule” Area for better productivity.

- * *Flip Chip Area* : “Fine Rule” Area
- * *Outside Flip Chip Area* : “Regular Rule” Area



3-1 Flip Chip Area (Fine Design Rule Area)

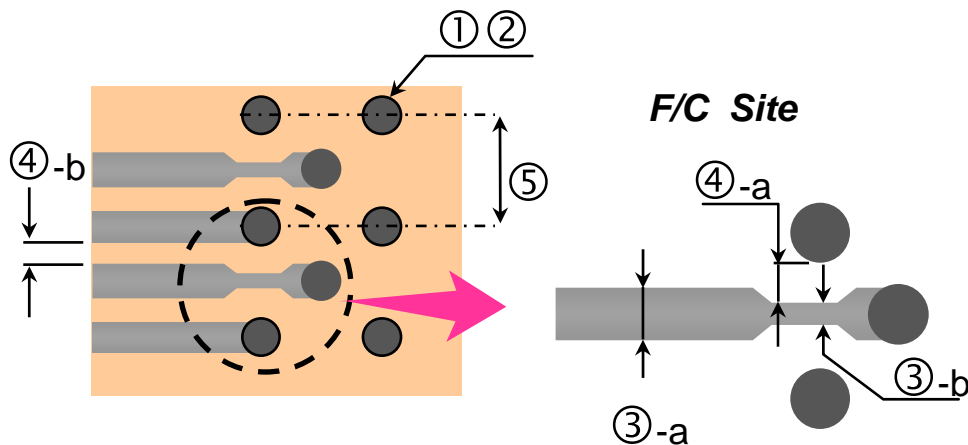
3-1-1 F/C Pad



UNIT:μm

Design Parameter	Production	Pilot
① Pad (Via) Pitch	≥ 180	≥ 150
② Pad (Via) Diameter	≥ 70	≥ 60

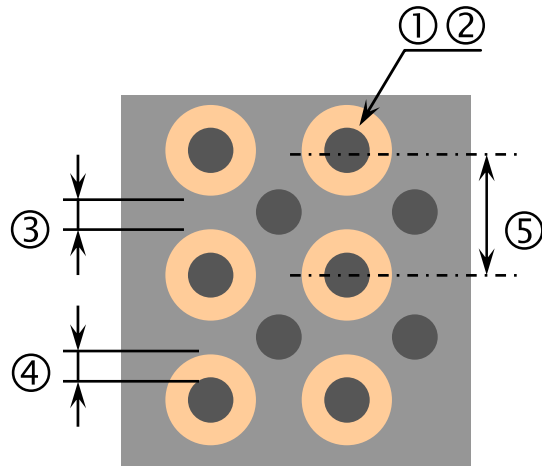
3-1-2 Signal Line



UNIT:μm

Design Parameter	Production	Pilot
① Via Diameter	≥ 70	≥ 60
② Cover Pad	≥ 70	≥ 60
③ -a Line Width	≥ 60	≥ 55
③ -b Line Width (between vias)	≥ 40	≥ 35
④ -a Isolation Gap (via to line)	≥ 60	≥ 55
④ -b Isolation Gap (line to line)	≥ 60	≥ 55
⑤ Via Pitch	≥ 230	≥ 205

3-1-3 PWR / GND Plane

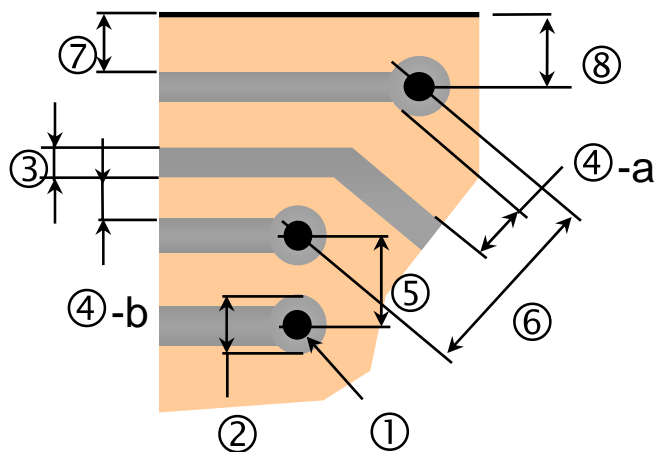
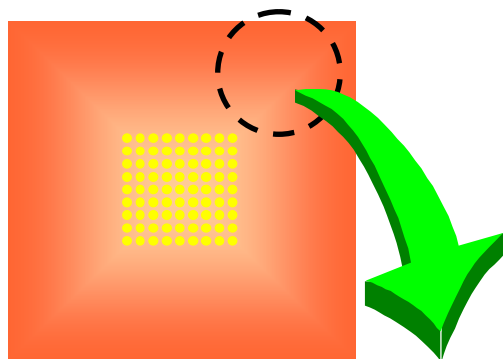


UNIT; μm

Design Parameter	Production	Pilot
① Via Diameter	≥ 70	≥ 60
② Cover Pad Diameter	≥ 70	≥ 60
③ Metal Path width	≥ 30	≥ 25
④ Isolation Gap	≥ 60	≥ 55
⑤ Via Pitch with Metal	≥ 220	≥ 195

3-2 Outside Flip Chip Area (Regular Design Rule Area)

3-2-1 Signal Line

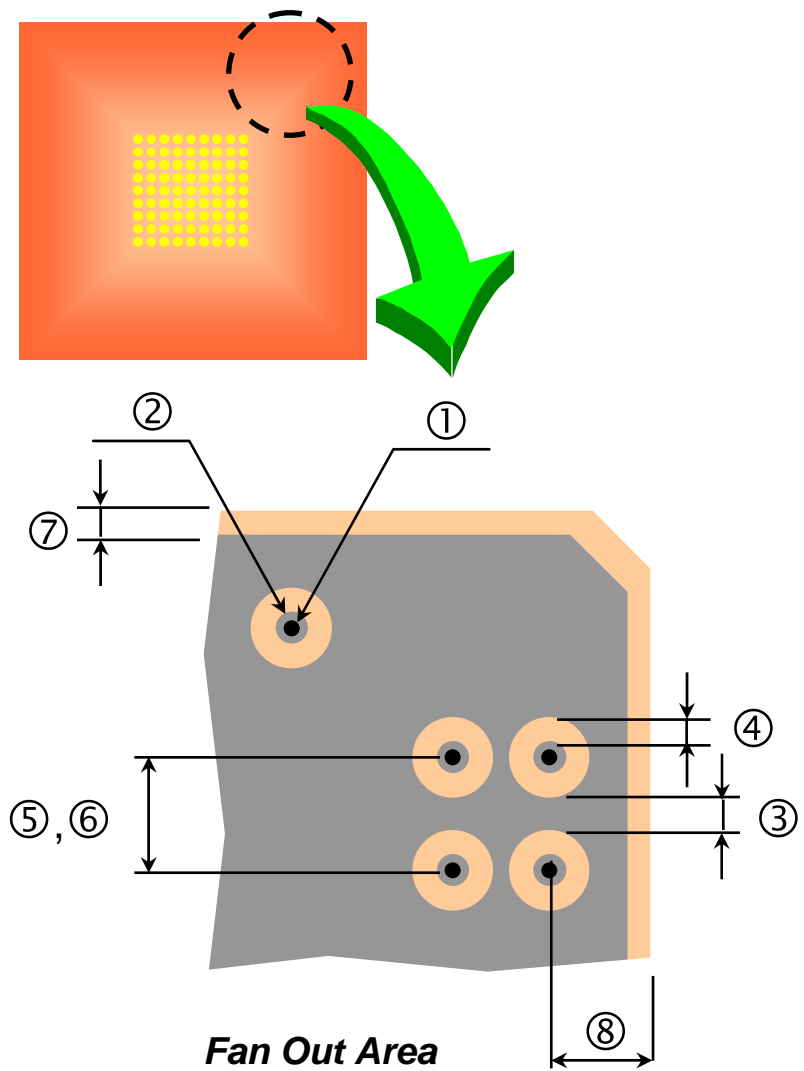


Another Site

UNIT : μm

Design Parameter	Standard	Special
① Via Diameter	≥ 150	≥ 100
② Cover Pad Diameter	≥ 250	≥ 100
③ Line Width	≥ 100	≥ 75
④ -a Isolation Gap(pad to line)	≥ 150	≥ 120
④ -b Isolation Gap (line to line)	≥ 150	≥ 100
⑤ Via Pitch	≥ 640	≥ 250
⑥ Via Pitch with 1 Line $\text{②} + \text{③} - \text{b} + 2 \times \text{④} - \text{a}$	≥ 650	≥ 415
⑦ Ceramic Edge to Line	≥ 640	≥ 300
⑧ Ceramic Edge to Via	≥ 640	≥ 380

3-2-2 PWR / GND Plane

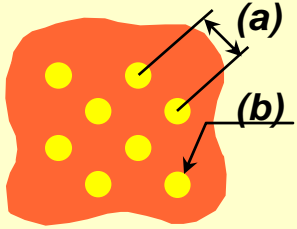


UNIT : μm

Design Parameter	Standard	Special
① Via Diameter	≥ 150	≥ 100
② Cover Pad Diameter	≥ 250	≥ 100
③ Width of Metal between Vias	≥ 150	≥ 75
④ Isolation Gap (pad to Plane)	STD tape	≥ 150
	Less than 5 mil tape	≥ 225
⑤ Via Pitch	≥ 640	≥ 250
⑥ Via Pitch with Metal $② + ③ + 2 \times ④$	STD tape	≥ 475
	Less than 5 mil tape	≥ 625
⑦ Ceramic Edge to Plane	≥ 760	≥ 640
⑧ Ceramic Edge to Via	≥ 640	≥ 380

4. Design Rule Road Map

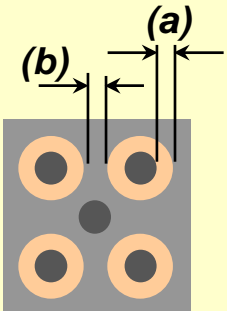
4-1 Flip Chip Pad

Items		Design value	'05	'06		'07	
			2H	1H	2H	1H	2H
	(a) Pitch	~200 μ m	Production High Productivity				
		~180 μ m	Production				
		~150 μ m	Pilot		Production		
		~130 μ m				Pilot	
	(b) Via Dia	100 ~ 95 μ m	Production High Productivity				
		70 μ m	Production				
		60 μ m	Pilot		Production		
		60 ~ 50 μ m				Pilot	

4-2 Signal

Items	Design value	'05	'06		'07	
		2H	1H	2H	1H	2H
 (a) Min Gap (Via ~ Line)	$\geq 90\mu\text{m}$	Production	High Productivity			
	$\geq 60\mu\text{m}$	Production				
	$\geq 55\mu\text{m}$	Pilot	Production			
	$\geq 50\mu\text{m}$		Pilot	Production		
	50~30 μm			Pilot		
 (b) Line Width (neck down)	$\geq 50\mu\text{m}$	Production	High Productivity			
	$\geq 40\mu\text{m}$	Production				
	$\geq 35\mu\text{m}$	Pilot	Production			
 (c) Line Width / (d) Space (routing)	$\geq 75 / 75\mu\text{m}$	Production	High Productivity			
	$\geq 60 / 60\mu\text{m}$	Production				
	$\geq 55 / 55\mu\text{m}$	Pilot	Production			
	$\geq 50 / 50\mu\text{m}$		Pilot	Production		
	50~30 / 50~30 μm			Pilot		

4-3 PWR/GND Plane

Items		Design value	'05	'06		'07	
			2H	1H	2H	1H	2H
	(a) Min Gap (Via ~ Metal)	$\geq 90\mu\text{m}$	Production	High Productivity			
		$\geq 60\mu\text{m}$	Production				
		$\geq 55\mu\text{m}$	Pilot	Production			
		$\geq 50\mu\text{m}$		Pilot	Production		
		50~30 μm				Pilot	
	(b) Metal Width	$\geq 50\mu\text{m}$	Production	High Productivity			
		$\geq 30\mu\text{m}$	Production				
		$\geq 25\mu\text{m}$	Pilot	Production			
		$\geq 20\mu\text{m}$		Pilot	Production		