



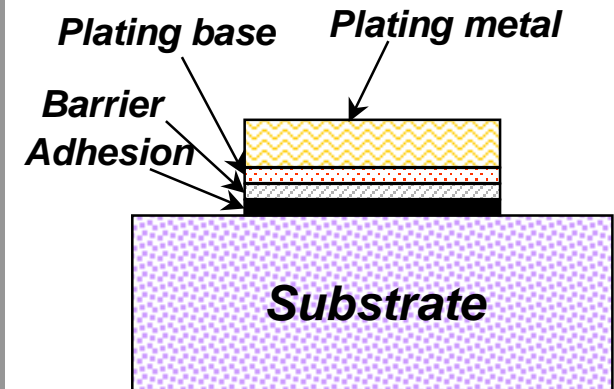
Thin Film Application

- 1. Single layer*
- 2. Multi-layer (Copper- Polyimide)*

1. Single Layer Thin Film

1.1 Metal construction for single layer thin film

Application		Thin film metal by sputtering			Plating Metal
		Adhesion	Barrier	Plating base	
General Conductor	for Wire Bonding and Soldering	Ti	---	Cu	Cu-Ni-Au
	For Wire Bonding	Ti	---	Pd	Au
	for Ag/Cu brazing (High temp. resistant)	Ti	Mo	Cu	Cu-Ni-Au
		Ti	---	Mo	Ni-Au
w/ Thin film Resistor	for Wire Bonding and Soldering	Ta ₂ N	Ti or Cr	Cu	Cu-Ni-Au
	For Wire Bonding	Ta ₂ N	Ti or Cr	Pd	Au

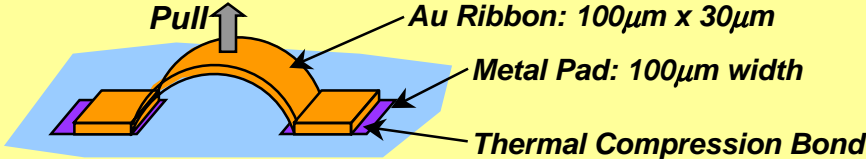
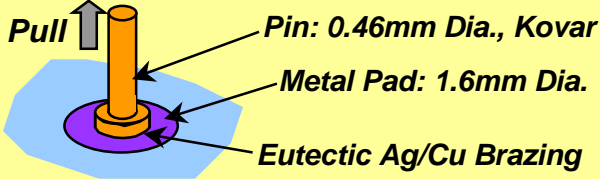




1.2 Outline of single layer thin film

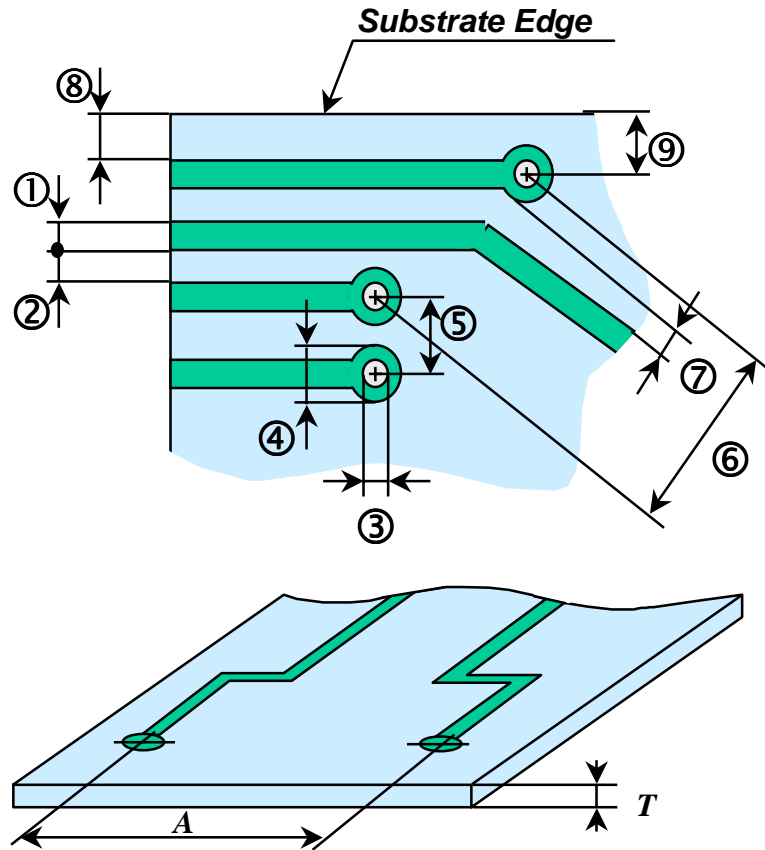
Item	Capability	Condition
Pattern Definition - Line Width - Line Spacing	<Standard> / <special> 75 μ m Min. / 50 μ m Min. 40 μ m Min. / 30 μ m Min.	
Metal Thickness	2 ~ 15 μ m (Optional)	By electrolytic plating
Thin Film Resistor - Resistor Film - Sheet Resistance - Resistor Size - Resistance Tolerance w/o Trimming (R size) w/ Trimming (R size)	Tantalum nitride (Ta ₂ N) 10 ~ 50 Ω /SQ. 100 μ mSQ. Min. +/-10% (R \geq 200mm SQ.) +/-20% (R <200mm SQ.) +/-2% (R \geq 200mm SQ.) +/-5% (R <200mm SQ.)	Substrate : Alumina or AlN Trimming : YAG Laser

1.3 Characteristics of single layer thin film

Item	Characteristics	Condition
Sheet Resistance	< 5 mΩ/SQ.	5 μm thk. of Cu or Au plating
Metal Adhesion	> 50 N/mm ² (Pull strength of Au ribbon)	
	> 80 N/mm ² (Pull strength of brazed pin)	
	Reliability: No degradation after: Temp. Cycle Test (TCT), and Pressure Cooker Test (PCT)	TCT: MIL-STD-883, cond.C - 1000Hrs PCT: 120 C, 85%RH(1.7atm) - 1000Hrs
Stability of Thin Film Resistor	Resistance Change: < 0.1% (w/o trimming) < 0.4% (w/ trimming)	High Temp. Aging, 150C in air - 1000Hrs, and High Temp.+High Humid., 85C+85%RH - 1000Hrs

1.4 Design rule of single layer thin film metallization

Thin film metallization on the cofired ceramic substrate



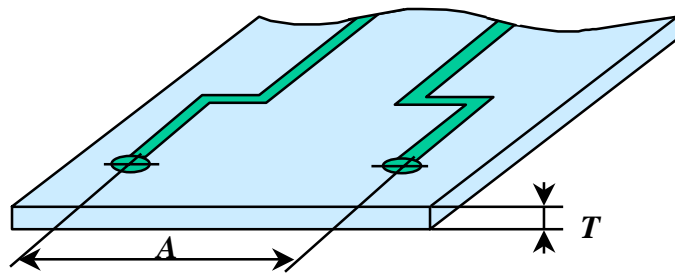
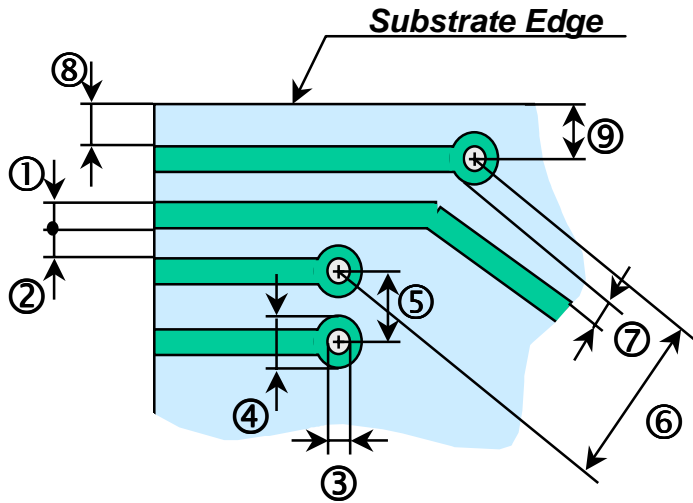
A : Maximum Via Pitch

UNIT: mm

Location		Low Cost	Standard
①	Line Width	≥ 0.076	≥ 0.051
②	Line to Line Spacing	≥ 0.051	≥ 0.038
③	Via Diameter	≥ 0.152	≥ 0.102
④	Via Cover Pad Diameter	$③+(Ax0.8\%) +0.102$	$③+(Ax0.8\%) +0.102$
⑤	Via Pitch	≥ 0.635	≥ 0.254
⑥	Via Pitch (w/ 1 Line spacing)	$①+④+⑦x2$	$①+④+⑦x2$
⑦	Via Cover Pad to Line	≥ 0.041	≥ 0.030
⑧	Subst. Edge to Line Spacing	≥ 0.508	≥ 0.406
⑨	Subst. Edge to Via Spacing	≥ 0.635	≥ 0.381

Thin film metallization on the plain ceramic substrate

UNIT: mm



A : Maximum Via Pitch

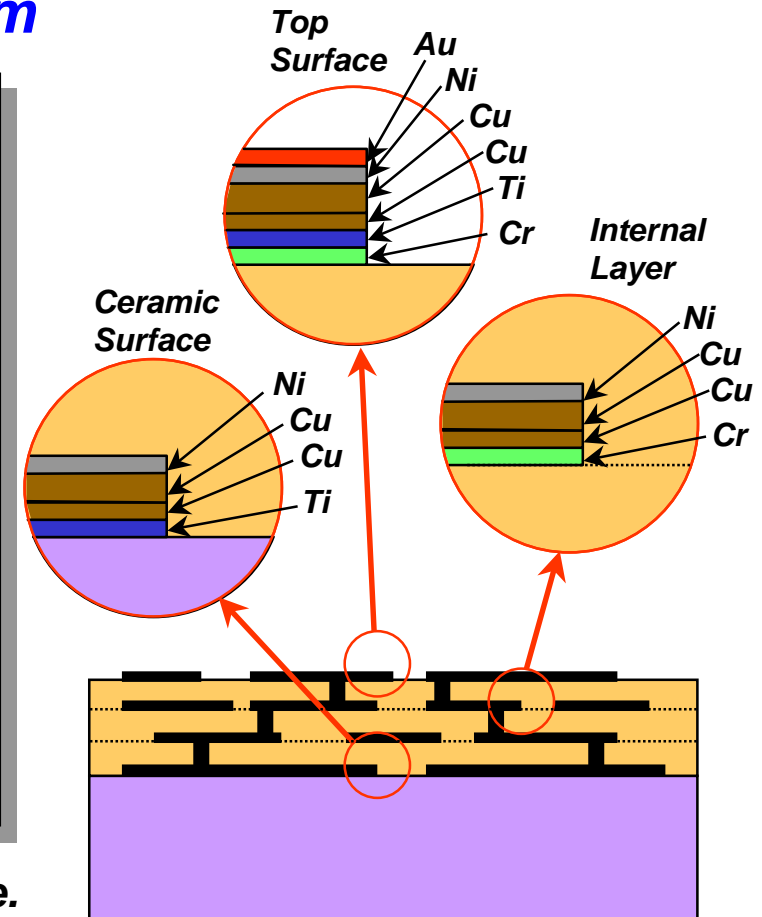
Location		Low Cost	Standard
①	Line Width	≥ 0.076	≥ 0.051
②	Line to Line Spacing	≥ 0.051	≥ 0.038
③	Via Hole Dia.		
	Punched Via	$\geq T, NLT \pm 0.152$	$\geq T/3, NLT \pm 0.203$
	Lasered Via	$\geq T, NLT \pm 0.254$	$\geq T/3, NLT \pm 0.203$
④	Via Hole Cover Pad Dia.		
	Punched Via	$\geq ③ + 0.008A + 0.102$	$\geq ③ + 0.005A + 0.102$
	Lasered Via	$\geq ③ + 0.102$	$\geq ③ + 0.102$
⑤	Via Hole Pitch		
	Punched Via	≥ 0.635	≥ 0.254
	Lasered Via	$\geq ③ + T + 0.102$	$\geq ③ + T$
⑥	Via Hole Pitch (w/ 1 Line Spacing)	$① + ④ + ⑦ \times 2$	$① + ④ + ⑦ \times 2$
⑦	Via Cover Pad to Line Spacing	≥ 0.041	≥ 0.030
⑧	Subst. Edge to Line Spacing	≥ 0.508	≥ 0.406
⑨	Subst. Edge to Via Spacing	≥ 0.635	≥ 0.381

2. Multi-layer Thin Film

2.1 Metal construction for multilayer thin film

Application		Thin film metal by sputtering			Plating Metal
		Adhesion	Barrier	Plating base	
Top Surface		Cr	Ti	Cu	Cu-Ni-Au
Internal Layer		Cr	---	Cu	Cu-Ni
Ceramic Surface	Standard	Ti	---	Cu	Cu-Ni(-Cr*)
	w/ Resistor	Ta ₂ N	Ti/W	Cu	Cu-Ni(-Cr*)

Cr*(by sputtering) is required if metal pattern is solid plane.

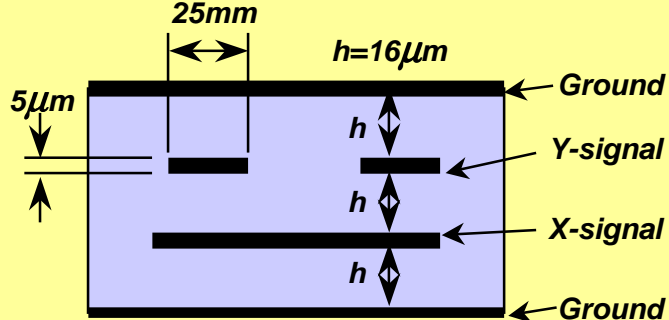
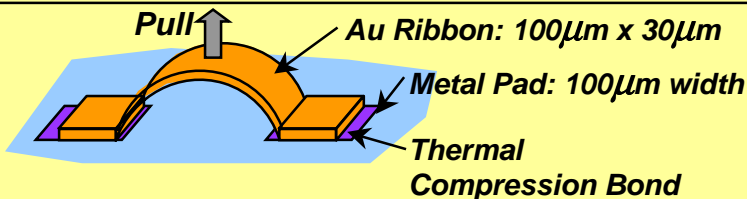




2.2 Outline of multilayer thin film

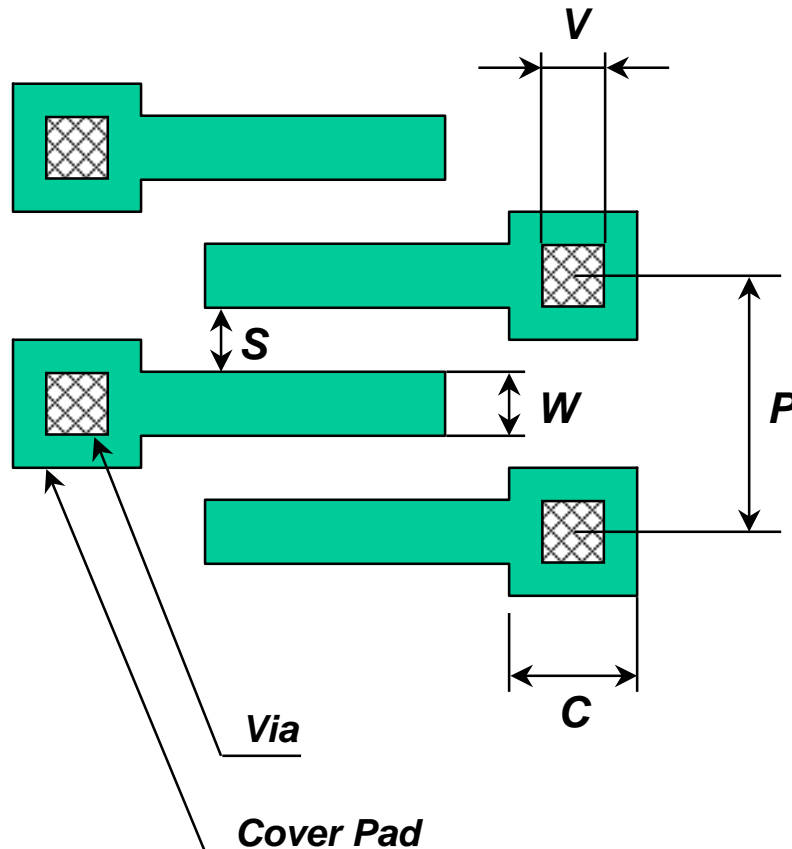
Item		Standard	Optional
Substrate	Material Size	Alumina (BA-914 , HA-995) 100 mmSQ.MAX.	AlN
# of Layers	Conductor Dielectric	≤ 6 Layers ≤ 6 Layers	≤ 8 Layers ≤ 8 Layers
Conductor	Metallization - Top Surface - Internal Layer - Bottom Layer Thickness Line Width / Spacing	Cr-Ti-Cu-Ni-Au Cr-Cu-Ni Ti-Cu-Ni ≤ 10 μm/Layer (by Request) 25μmMIN./50μmMIN.	Cr-Pd-Au Ti-Cu-Ni-Cr 15μmMIN./30μmMIN.
Via	Size / Pitch	50μm/150μmMIN. (filled & stacked via)	50μm/100μmMIN. (filled & staggered via)
Dielectric	Material Thickness Dielectric Constant/ Loss	Polyimide 10~25μm/Layer (by Request) 3.2/0.002 (@1MHz)	

2.3 Characteristics of multilayer thin film

Item	Characteristics	Condition
Line Resistance	1.5 Ω/cm	Line width/thickness: 25 μm /5 μm
Via Resistance	< 1m Ω	Via size: 50 μm SQ.
Insulation Resistance	> 10 ¹⁰ Ω	Plane to plane (18mm x 13mm) PI thickness: 25 μm
Line Capacitance	1.2 pF/cm	Dual strip line structure ($Z_0=50\Omega$) 
Propagation Delay	60 ps/cm	
Cross Talk Noise	11% @line spacing 20 μm 6% @line spacing 30 μm 4% @line spacing 50 μm	
Insertion Loss	- 0.6 dB/cm @ 1GHz - 1.6 dB/cm @ 10GHz	
Metal Adhesion	> 50N/mm ²	

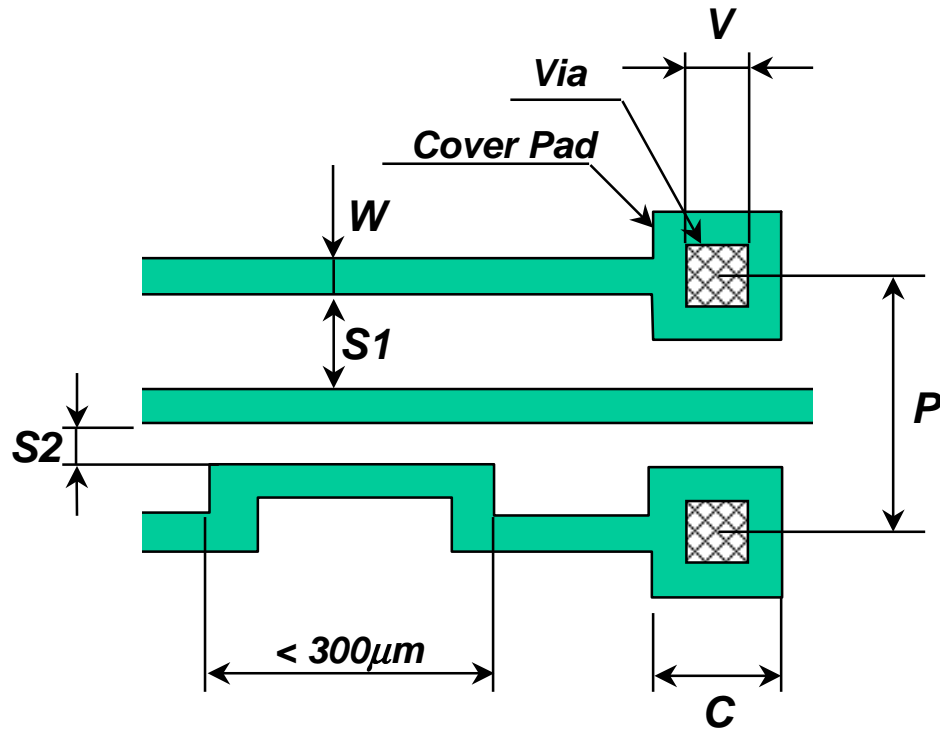
2.4 Design rule of multilayer thin film metallization

Top surface metallization



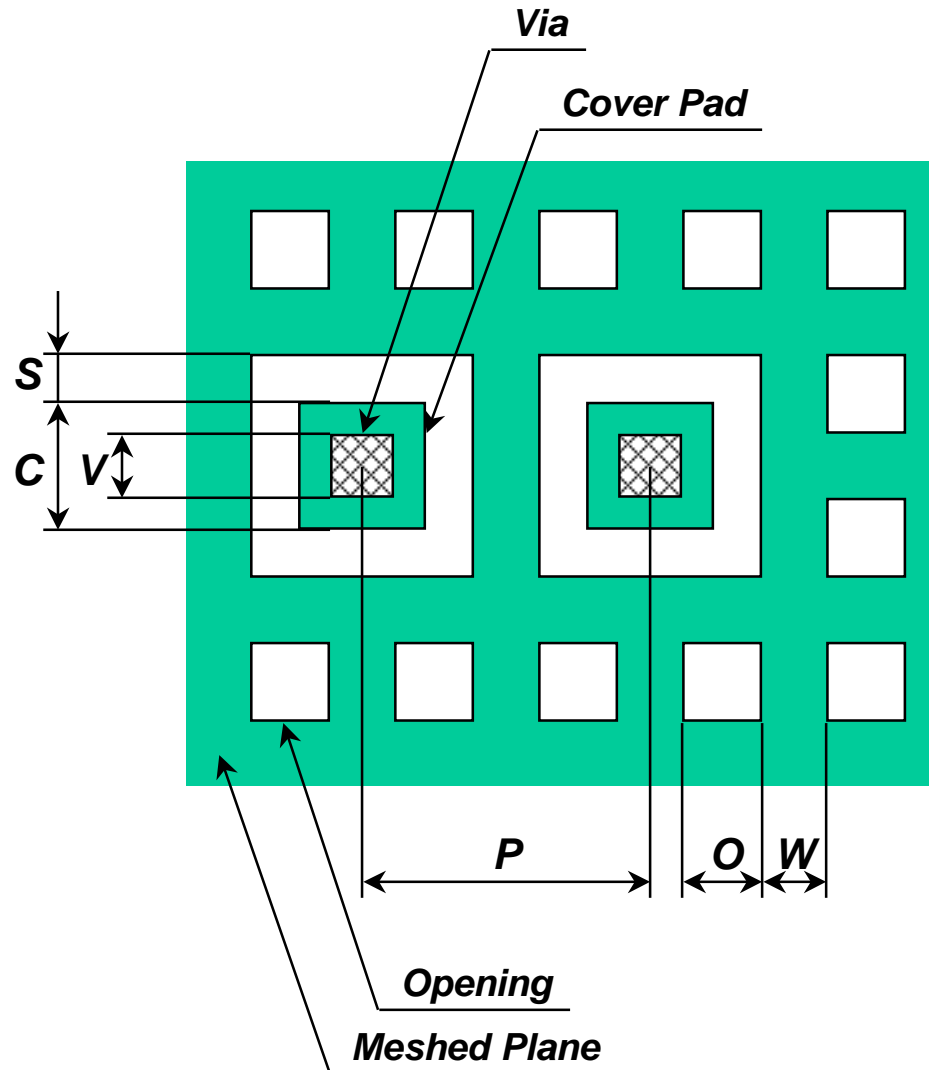
Location		Rule
W	Pad Width	$\geq 50 \mu\text{m}$
S	Pad Spacing	$\geq 50 \mu\text{m}$
V	Via Size (Filled Via)	$50 \mu\text{m}$
P	Via Pitch (Stacked Via)	$\geq 150 \mu\text{m}$
	(Staggered Via)	$\geq 100 \mu\text{m}$
C	Cover Pad Size	$\geq (V+20) \mu\text{m}$

Internal trace (signal layer)



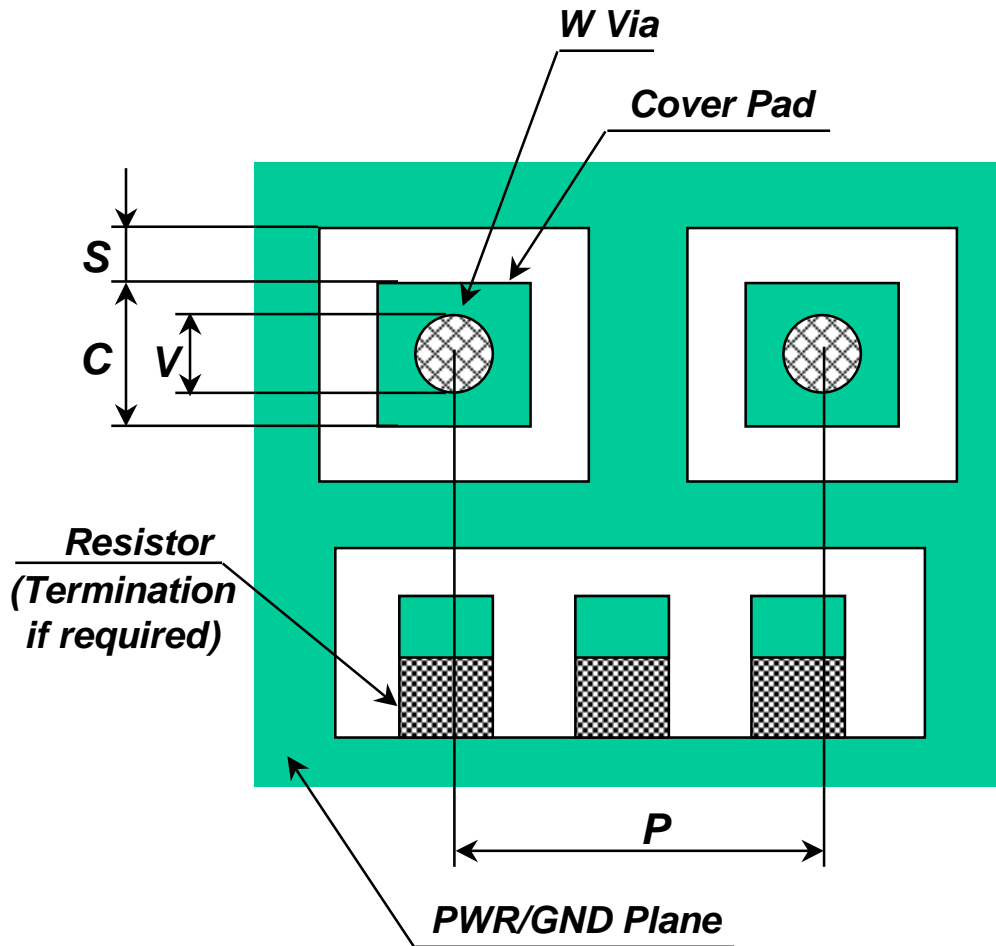
Location		Rule
W	Line Width	$\geq 25 \mu\text{m}$
S	Metal Spacing S1: Length $\geq 300\mu\text{m}$ S2: Length $< 300\mu\text{m}$	$\geq 50 \mu\text{m}$ $\geq 30 \mu\text{m}$
V	Via Size (Filled Via)	$50 \mu\text{m}$
P	Via Pitch (Stacked Via) (Staggered Via)	$\geq 150 \mu\text{m}$ $\geq 100 \mu\text{m}$
C	Cover Pad Size	$\geq (V+20) \mu\text{m}$

Internal plane (GND/PWR)



Location		Rule
W	Mesh Width	$\geq 50 \mu m$
O	Opening Size	$\geq W$
S	Clearance	$\geq 50 \mu m$
V	Via Size (Filled Via)	$50 \mu m$
P	Via Pitch (Stacked Via)	$\geq 150 \mu m$
	(Staggered Via)	$\geq 100 \mu m$
C	Cover Pad Size	$\geq (V+20) \mu m$

Bottom layer (PWR/GND plane on the ceramic substrate)



	Location	Rule
S	Clearance	$\geq 100 \mu\text{m}$
V	Via Size	$\geq 100 \mu\text{m}$
C	Cover Pad Size <i>D: Maximum Via Pitch</i> <i>T: Shrinkage Tolerance (STD: T=0.5%)</i>	$\geq [V+(D \times T)]$
R	Resistor (Ta_2N)	$\geq 200 \mu\text{m}^2$