



## COMMUNICATION MEDIA COMPONENTS GROUP

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NGK SPARK PLUG CO.,LTD  
2808,IWASAKI,KOMAKI,AICHI,485,JAPAN

*REV.1 / May / 2005*

***- LTCC (NOC) Flip Chip Package -***

# ***General Design Guide***



Material properties

**NOC (Non Crystallized Glass System)**

Material		LTCC NOC	HTCC (REF)
Conductor		Cu	W.Mo
Dielectric constant [3,6,12GHz] Perturbation Method [40GHz] Cavity Resonance Method	3GHz	5.9	9.2
	6GHz	5.8	9.2
	12GHz	5.6	9.2
	40GHz	6.0	9.2
Dielectric loss	3 GHz	0.0006	0.0005
	6 GHz	0.0012	0.0009
	12 GHz	0.0016	0.0010
	40 GHz	0.0022	0.0015
C.T.E.[ ppm/deg.C]		5.2	7.6
Thermal Conductivity [ W mK]		3	17
Flexural Strength [MPa]		250	350
Young's Modulus* [GPa]		105	280
Poisson's ratio*		0.21	0.23
Fracture toughness KIC [MPam <sup>-0.5</sup> ]		2.4	3.0
Note		Pb free	Pb free
Availability		Development	HVM



## Metallization

1. **Metallization Resistivity** : **1.9mOHM/sq** (*calculation value at 16umt*)

2. **Via Resistivity** : **4.0 u OHM c**

3. **Metallization Thickness \*** : **Signal = 16umt**  
**GND = 10umt**  
**BGA pad = 23umt**

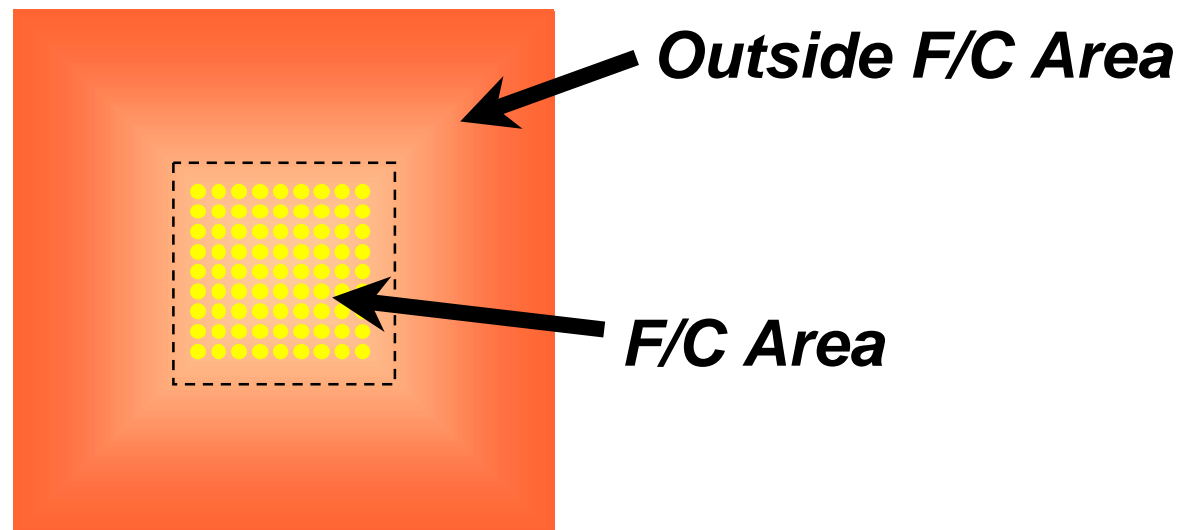
**\* After Firing Thickness**

4. **Metallization Thickness Tolerance** : **+/- 5 um**  
**(after Firing/ estimated Value)**

## Internal Design Rule

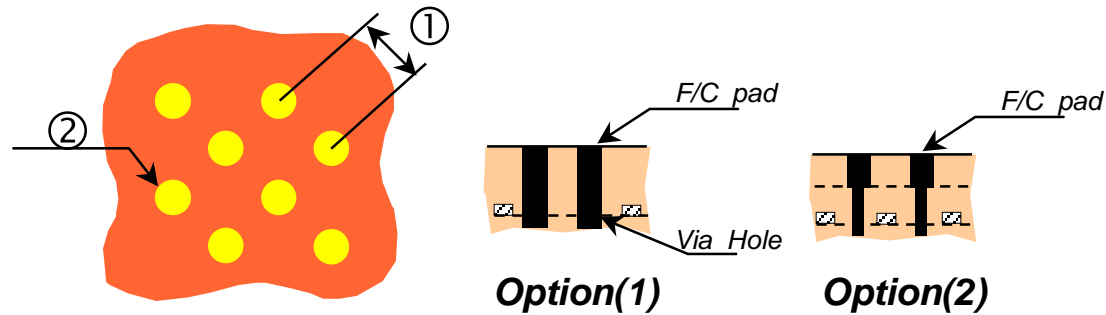
*Design Rules are separated into “Fine Rule” Area & “Regular Rule” Area for better productivity.*

- \* *Flip Chip Area* : “*Fine Rule*” Area
- \* *Outside Flip Chip Area* : “*Regular Rule*” Area



## 2-2. Flip Chip Area ( Fine Design Rule Area )

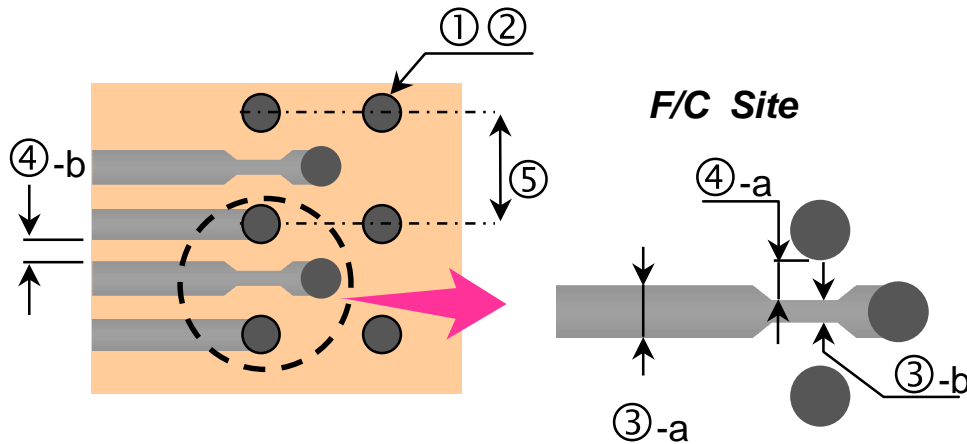
### 2-2-1 F/C Pad



UNIT :  $\mu\text{m}$

Design Parameter	Design Rule ( Pilot Only )
① Pad (Via) Pitch	$\geq 225$
② Pad (Via) Diameter (Tolerance)	$\geq 100$ (+/-25)

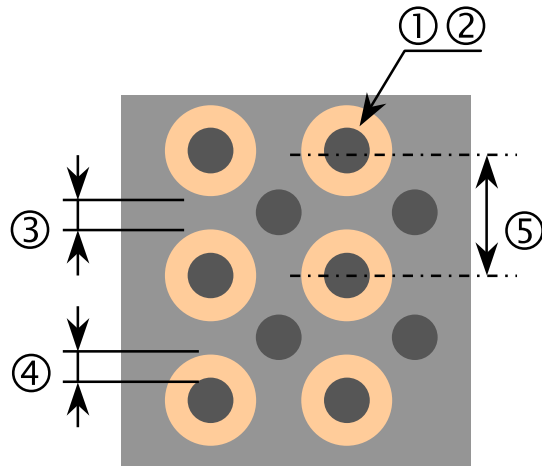
### 2-2-2 Signal Line



UNIT :  $\mu\text{m}$

Design Parameter	Design Rule ( Pilot Only )
① Via Diameter	$\geq 100$
② Cover Pad	$\geq 100$
③ -a Line Width	$\geq 75$
③ -b Line Width (between vias)	$\geq 50$
④ -a Isolation Gap (via to line)	$\geq 50$
④ -b Isolation Gap (line to line)	$\geq 75$
⑤ Via Pitch	$\geq 250$

### 2-2-3 PWR / GND Plane

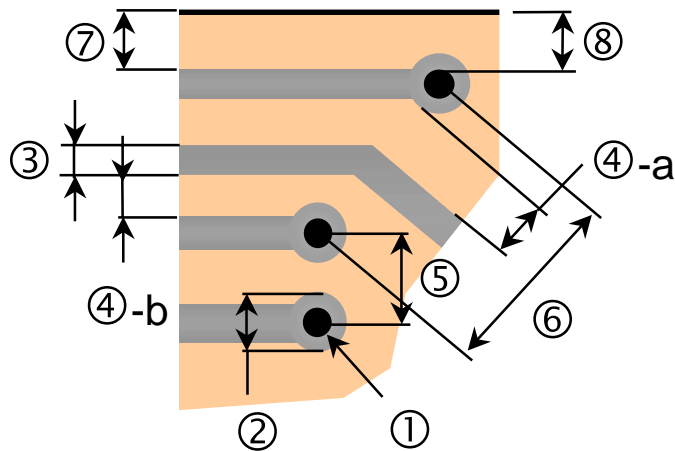
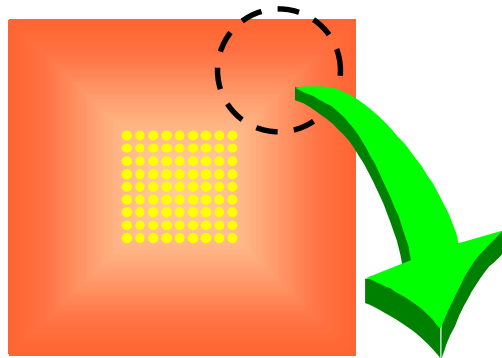


UNIT :  $\mu\text{m}$

Design Parameter	Design Rule ( Pilot Only )
① Via Diameter	$\geq 100$
② Cover Pad Diameter	$\geq 100$
③ Metal Path width	$\geq 25$
④ Isolation Gap	$\geq 50$
⑤ Via Pitch with Metal	$\geq 225$

## 2-3. Outside Flip Chip Area ( Regular Design Rule Area )

### 2-3-1 Signal Line

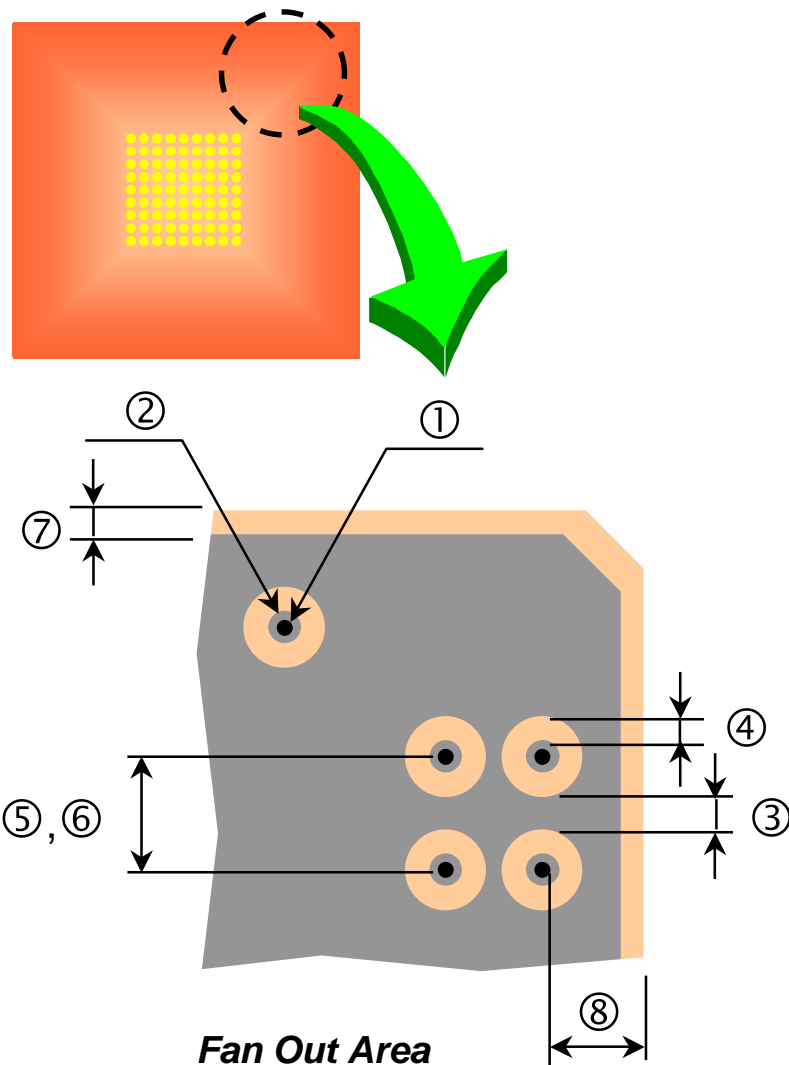


Another Site

UNIT :  $\mu\text{m}$

Design Parameter	Design Rule ( Pilot Only )
① Via Diameter	$\geq 100$
② Cover Pad Diameter	$\geq 100$
③ Line Width	$\geq 100$
④ -a Isolation Gap (pad to line)	$\geq 120$
④ -b Isolation Gap (line to line)	$\geq 100$
⑤ Via Pitch	$\geq 250$
⑥ Via Pitch with 1 Line $\text{②} + \text{③} + 2 \times \text{④} - \text{a}$	$\geq 440$
⑦ Ceramic Edge to Line Edge	$\geq 500$
⑧ Ceramic Edge to Via Edge	$\geq 500$

### 2-3-2 PWR / GND Plane



UNIT :  $\mu\text{m}$

Design Parameter		Design Rule ( Pilot Only )
①	Via Diameter	$\geq 100$
②	Cover Pad Diameter	$\geq 100$
③	Width of Metal between Vias	$\geq 75$
④	Isolation Gap (pad to Plane)	STD tape $\geq 150$
		Less than 5 mil tape $\geq 225$
⑤	Via Pitch	$\geq 250$
⑥	Via Pitch with Metal $\text{②} + \text{③} + 2 \times \text{④}$	STD tape $\geq 475$
		Less than 5 mil tape $\geq 625$
⑦	Ceramic Edge to Plane Edge	$\geq 500$
⑧	Ceramic Edge to Via Edge	$\geq 500$