



COMMUNICATION MEDIA COMPONENTS GROUP

NGK SPARK PLUG CO., LTD.
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Rev. A / Apr.2004

NTK HTCC Package General Design Guide

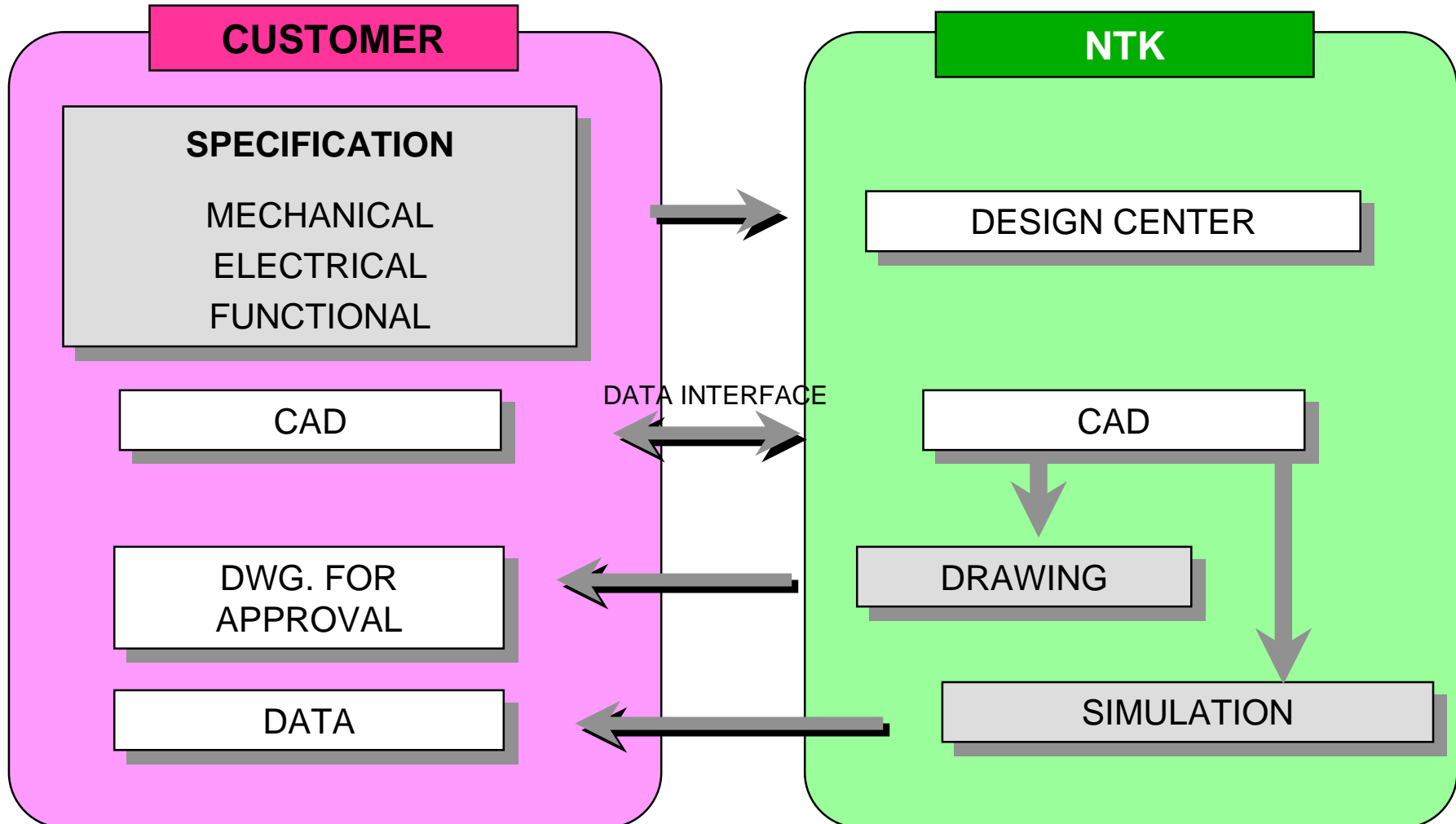


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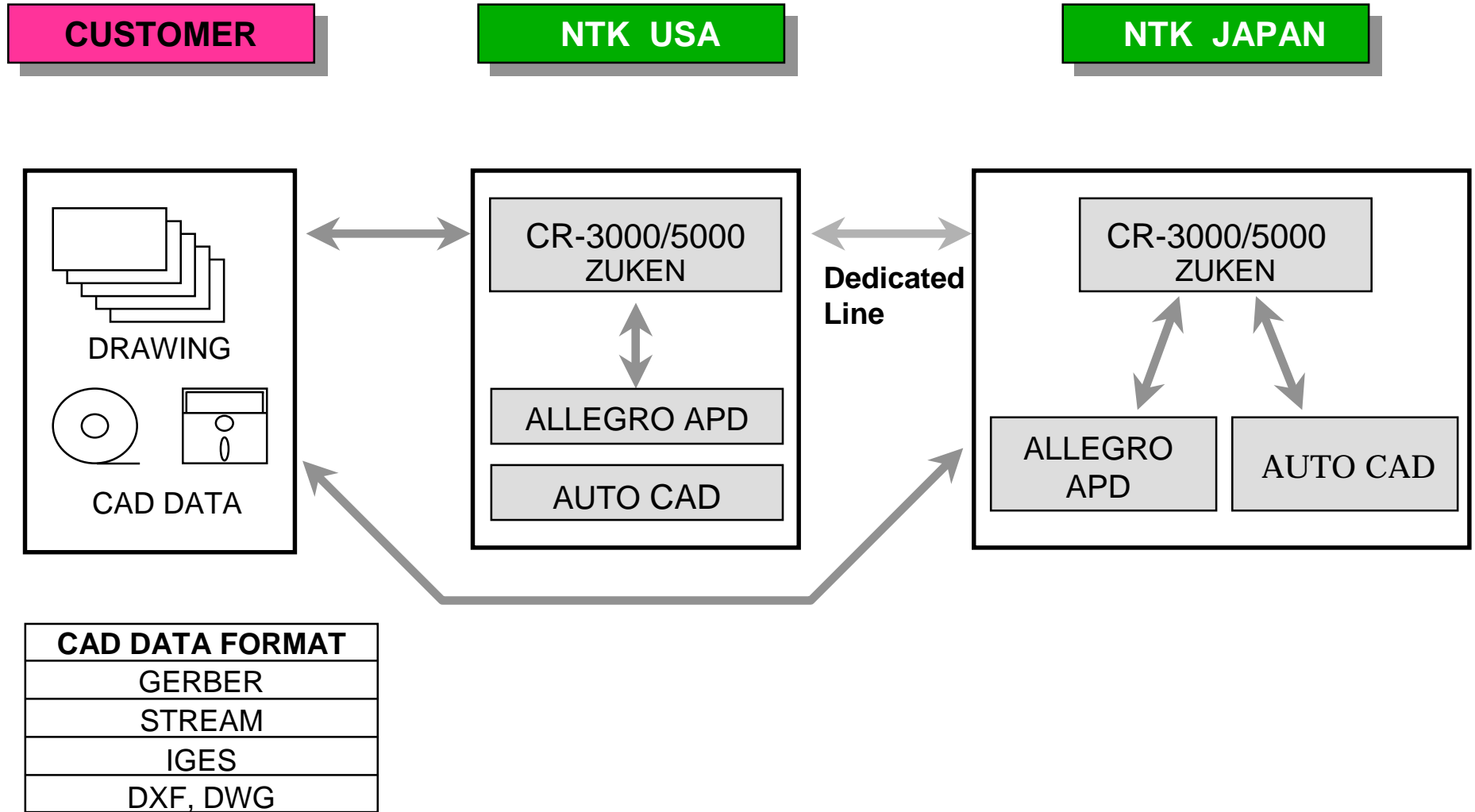
1. PACKAGE DESIGN

1.1 DESIGN PROCESS FLOW



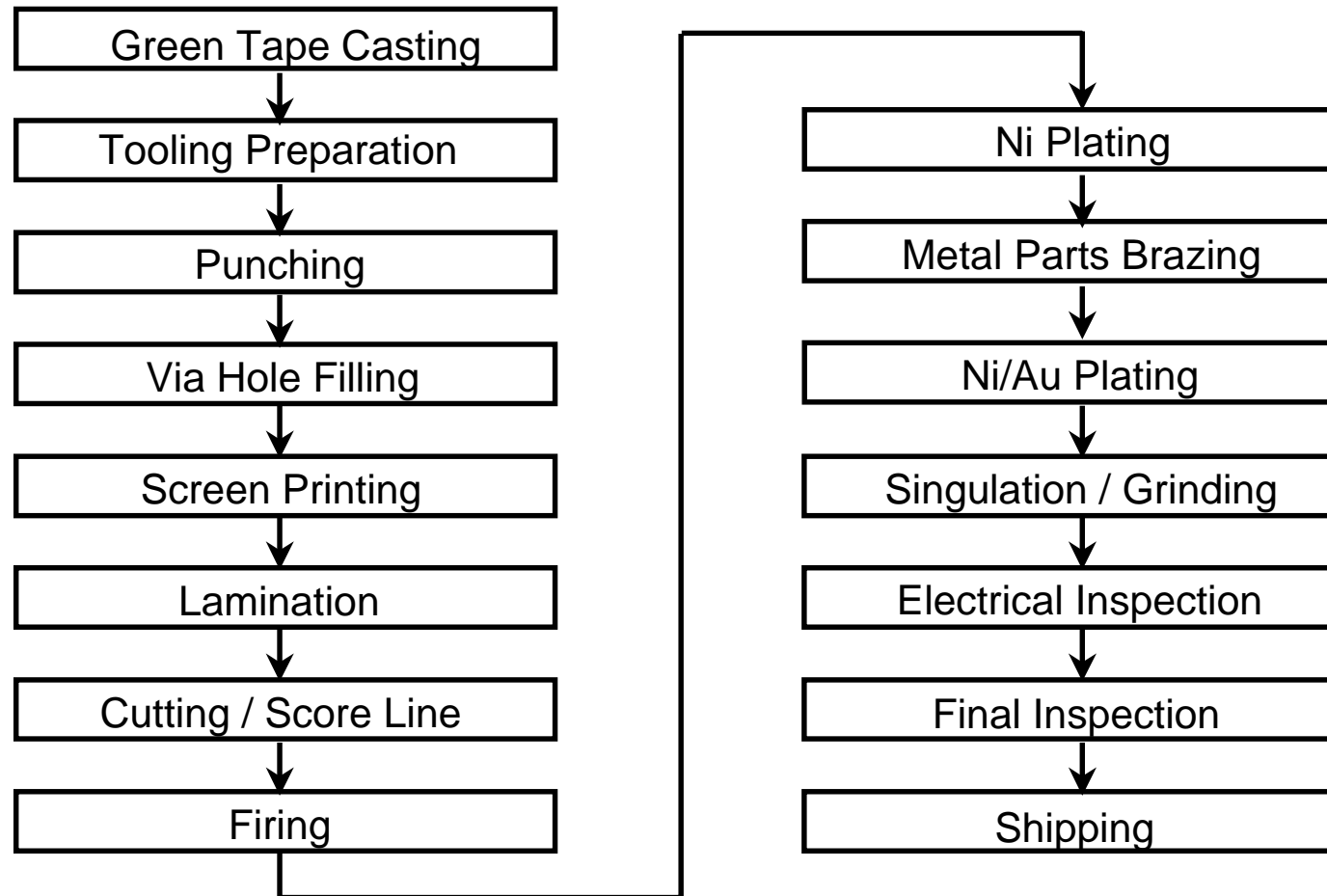


1.2 CAD SYSTEM

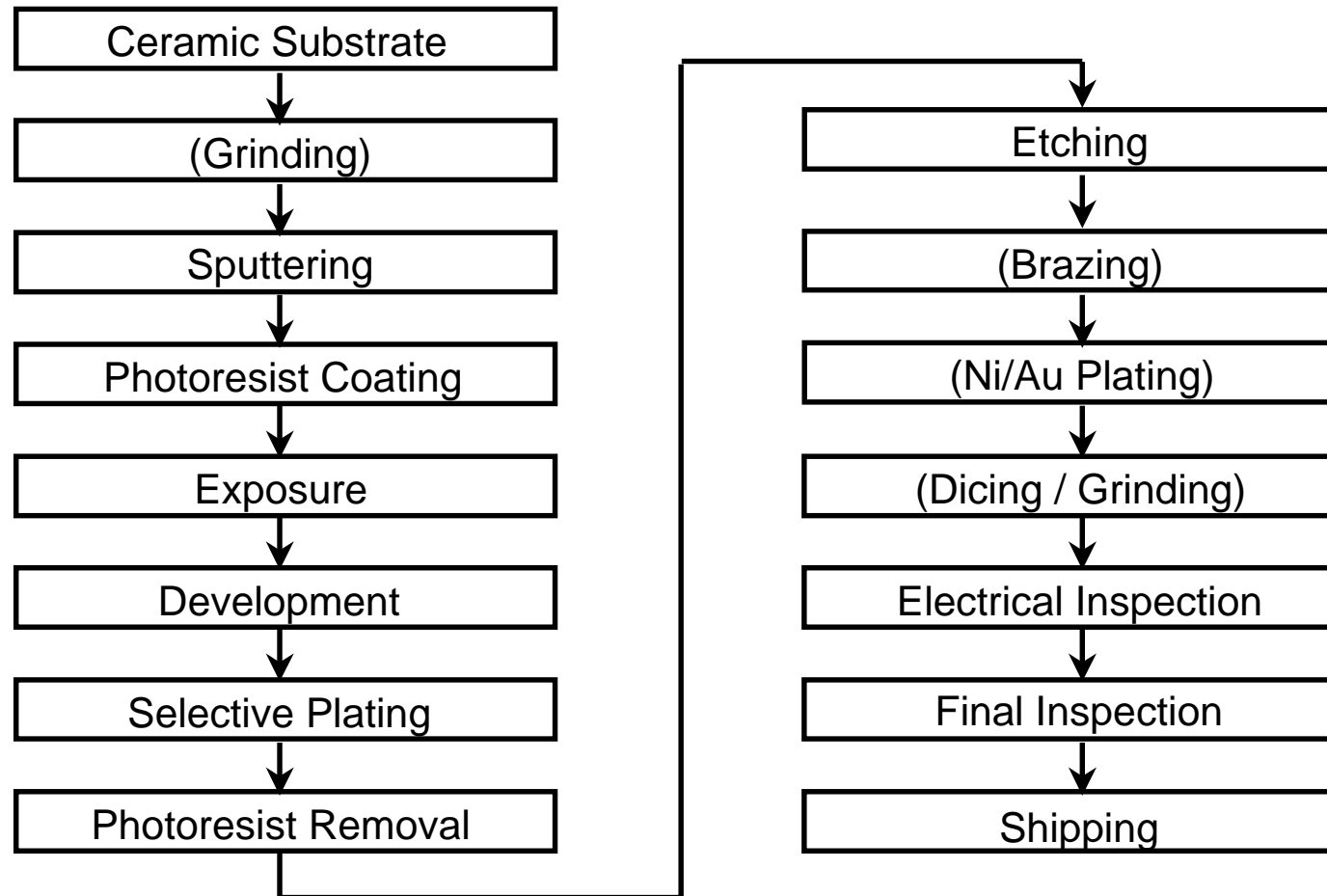


2. MANUFACTURING PROCESS FLOW (General)

2.1 COFIRED MULTILAYER PACKAGE



2.2 THIN FILM METALLIZATION





3. MATERIAL CHARACTERISTICS

3.1 CERAMIC MATERIAL

	Alumina		ALN	Polyimide (REF.)	Si (REF.)	GaAs (REF.)
	HA-921	BA-914				
T.C.E. [10 ⁻⁶ /K]	6.7 R.T.- 400C	6.8 R.T.- 400C	4.4 R.T.- 400C	20-70 R.T.- 300C	3.6 R.T.- 400C	6.0 R.T.- 400C
Thermal Conductivity [W/mK, R.T.]	17	17	170	0.2	125	54
Yung's Modulus [GPa]	280	280	350	3	—	—
Bending Strength [MPa]	350	350	350	—	100	—
α-Particle Count [Count/cm ² ·h]	< 0.1	< 0.1	< 0.1	—	—	—
Dielectric Constant 1MHz R.T. 10GHz R.T.	9.4 8.8	9.8 9.0	8.9 8.5	3.2 —	12.0 —	13.1 —
Dielectric Loss 1MHz R.T. 10GHz R.T.	5x10 ⁻⁴ 1x10 ⁻³	4x10 ⁻⁴ 1x10 ⁻³	3x10 ⁻⁴ 3x10 ⁻³	6x10 ⁻³ —	— —	— —
Volume Resistivity [Ωm]	>10 ¹²	>10 ¹²	>10 ¹²	>10 ¹²	10 ⁸	10 ⁻⁵ - 10 ⁻⁶
Breakdown Voltage [kV/mm]	15	15	15	300	—	—



3.2 METAL PARTS (HEAT SINK MATERIAL)

Material	Density [gram/cm ³]	Specific Heat [J/kg·K]	Thermal Conductivity [W/mK] (R.T.)	T.C.E. [x10 ⁻⁶ /C] (R.T.- 400C)
CuW (Cu 10% W 90%)	17.0	163	180	6.0
ALN	3.3	670	170	4.4
Cu	9.0	377	398	17.0
Si (Ref.)	2.3	670	125	3.5
Al ₂ O ₃ (Ref.)	3.6	795	17	6.8
Kovar (Ref.)	8.4	460	17	5.5



3.3 CONDUCTOR

3.3.1 COFIRED METALLIZATION

Item		Standard	Special
Sheet Resistance	Surface (w/ Ni-Au Plating)	7 mΩ/SQ. MAX 6 mΩ/SQ. NOM	5 mΩ/SQ. MAX 4 mΩ/SQ. NOM
	Internal	15 mΩ/SQ. MAX 10 mΩ/SQ. NOM	10 mΩ/SQ. MAX 8 mΩ/SQ. NOM
Via Resistance (200μm DIA. - 250μm THK.)		5 mΩ NOM	2 mΩ NOM
Line to Line Insulation Resistance (Line to Line Spacing: 100μm, @ 100V DC)		≥ 1x 10 ¹⁰ Ω	

3.3.2 THIN FILM METALLIZATION

Item	Standard
Sheet Resistance (w/ Cu or Au Plating 5μm THK.)	6 mΩ/SQ. NOM
Line to Line Insulation Resistance (Line to Line Spacing: 100μm, @ 100V DC)	≥ 1x 10 ⁹ Ω
Adhesion Strength	≥ 50 N/mm ²



4. DESIGN RULE FOR COFIRED MULTILAYER

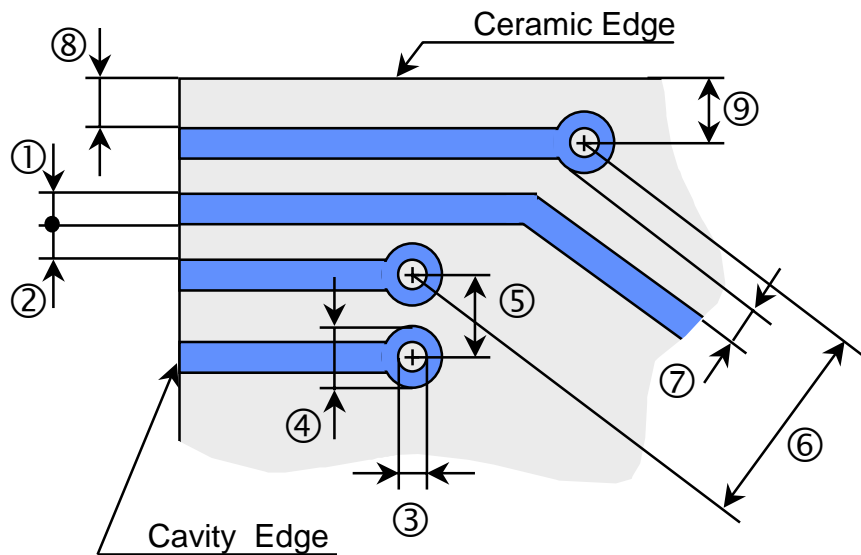
4.1 STANDARD PACKAGE

4.1.1 OUTLINE

UNIT: mm

Item		Standard	Special
Size		≤100 SQ	≤150 SQ
Layer Thickness		0.203 0.254 0.381 0.508 0.635 ≤ 5.08 Total	0.051 0.102 0.152 ≤ 10.16 Total
Layer Count		20	45
Tolerance	Outer Dimension	±0.8%, NLT±0.127	±0.5%, NLT±0.102
	Pattern Pitch	±0.8%, NLT±±0.051	±0.3%, NLT±0.051
	Thickness	±10%, NLT±0.051	±5%, NLT±0.038
	Cavity Dimension	±1.0%, NLT±0.127	±0.8%, NLT±0.102
Camber		0.102 / 25.4	0.051 / 25.4

4.1.2 EXPOSED SURFACE LAYER



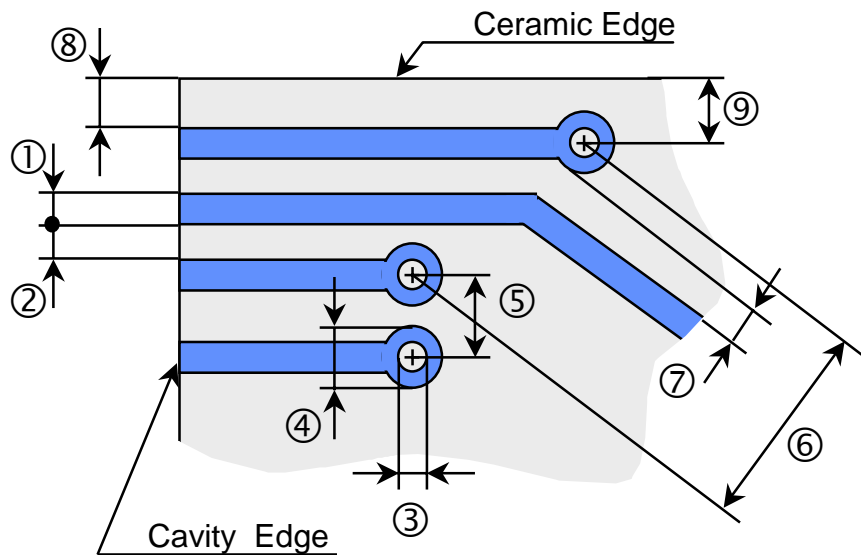
UNIT: mm

Location		Low Cost	Standard
①	Pad Width	≥0.203	≥0.102
②	Pad Spacing	≥0.203	≥0.051
③	Via Diameter	≥0.152	≥0.102
④	Via Cover Pad Diameter	≥0.406	≥0.203
⑤	Via Pitch	≥0.635	≥0.254
⑥	Via Pitch (w/ 1 Line Spacing)	①+②+⑦x2	①+②+⑦x2
⑦	Cover Pad to Line Spacing	≥0.254	≥0.102
⑧	Spacing A) Outer Edge to Line	≥0.508	≥0.406
	B) Cavity to Line	≥0.381	≥0.254
⑨	Spacing A) Outer Edge to Via	≥0.635	≥0.381
	B) Cavity to Via	≥0.635	≥0.508

4.1.3 BERIED CONDUCTOR LAYER

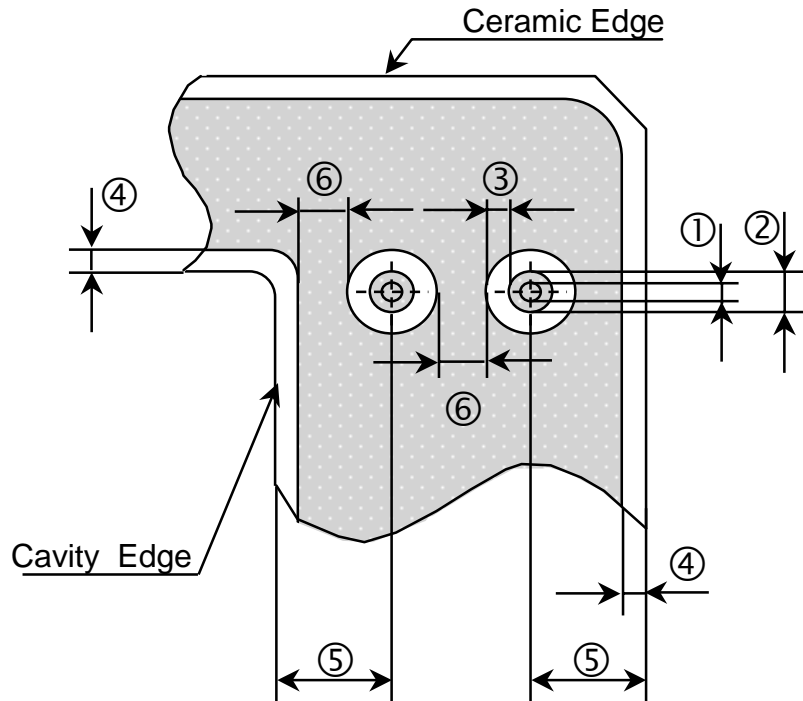
A. SIGNAL LAYER

UNIT: mm



Location		Low Cost	Standard
①	Line Width	≥0.203	≥0.102
②	Line Spacing	≥0.203	≥0.102
③	Via Diameter	≥0.203	≥0.102
④	Via Cover Pad Diameter	≥0.406	≥0.152
⑤	Via Pitch	≥0.635	≥0.254
⑥	Via Pitch (w/ 1 Line Spacing)	①+②+⑦x2	①+②+⑦x2
⑦	Cover Pad to Line Spacing		
	A) w/ Via from Upper Layer B) w/o Via from Upper Layer	≥0.305 ≥0.203	≥0.203 ≥0.152
⑧	Spacing		
	A) Outer Edge to Line B) Cavity to Line	≥0.635 ≥0.381	≥0.381 ≥0.254
⑨	Spacing		
	A) Outer Edge to Via B) cavity to via	≥0.635 ≥0.635	≥0.381 ≥0.508

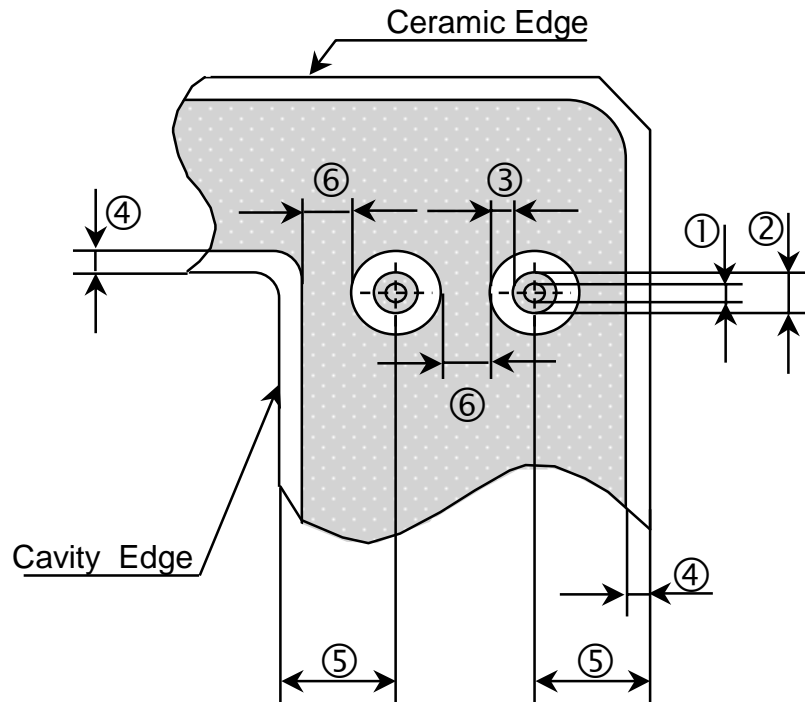
B. POWER / GROUND LAYER



UNIT: mm

Location		Low Cost	Standard
①	Via Diameter	≥0.203	≥0.102
②	Via Cover Pad Diameter	≥0.406	≥0.102
③	Clearance		
	A) w/ Via from Upper Layer B) w/o Via from Upper Layer	≥0.305 ≥0.203	≥0.152 ≥0.102
④	Spacing		
	A) Edge to Plane B) Cavity to Plane	≥0.762 ≥0.635	≥0.635 ≥0.508
⑤	Spacing		
	A) Outer Edge to Via B) Cavity to Via	≥0.635 ≥0.635	≥0.381 ≥0.508
⑥	Minimum Metal Width	≥0.152	≥0.076

C. CAPACITOR LAYER (2mil LAYER)



UNIT: mm

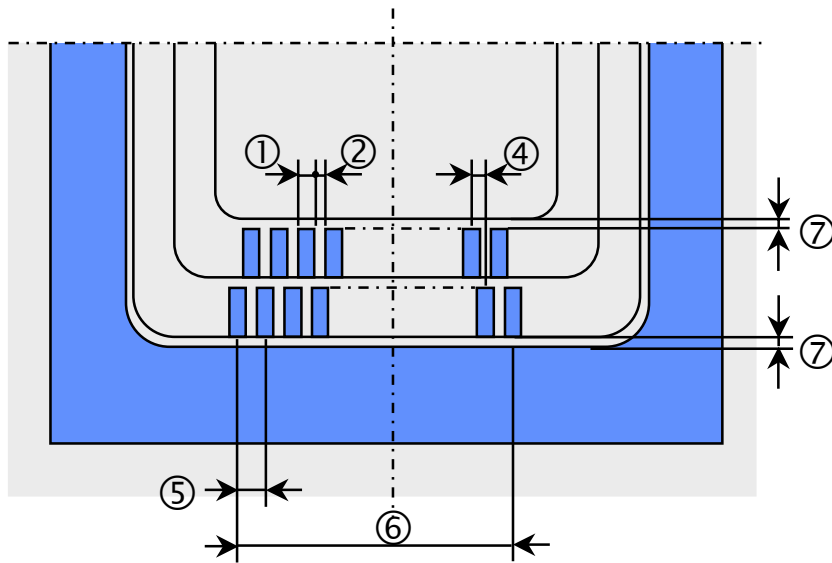
Location	Standard
① Via Diameter	≥ 0.203
② Via Cover Pad Diameter	≥ 0.406
③ Clearance A) w/ Via from Upper Layer B) w/o Via from Upper Layer	≥ 0.406 ≥ 0.406
④ Spacing A) Outer Edge to Plane B) Cavity to Plane	≥ 0.102 ≥ 0.635
⑤ Spacing A) Outer Edge to Via B) Cavity to Via	≥ 0.635 ≥ 0.635
⑥ Minimum Metal Width	≥ 0.203

<Capacitance Value>

1.4 nF/inch² (STD.)

2.1 nF/inch² (high-ε / US PAT. No.5099388)

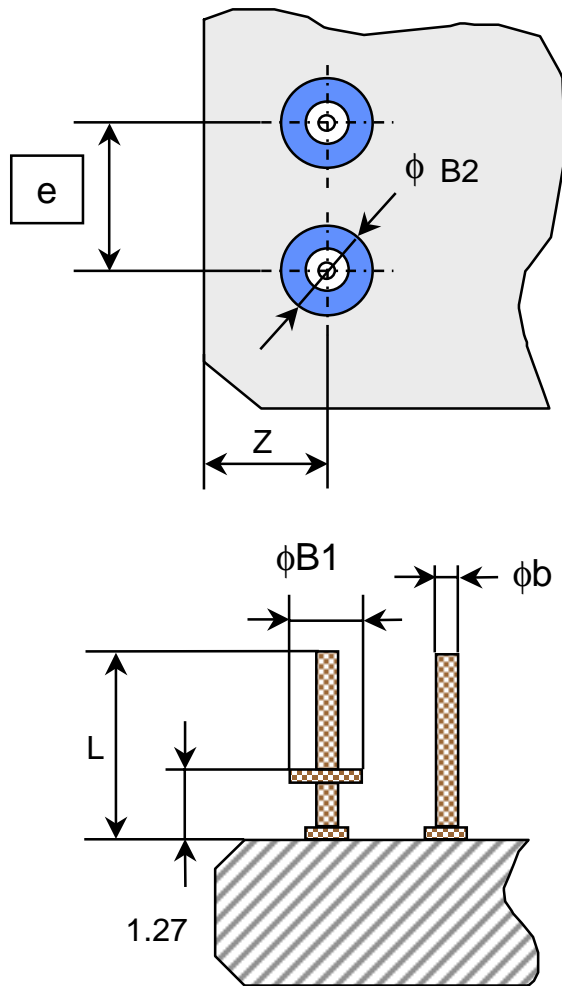
4.1.4 WIRE BONDING PAD



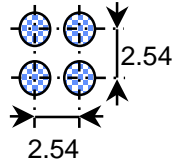
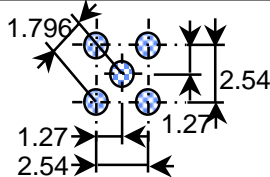
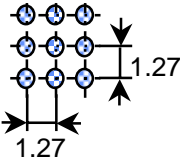
UNIT: mm

Location		Low Cost	Standard
①	Pad Width	≥ 0.203	≥ 0.102
②	Pad Spacing	≥ 0.203	≥ 0.051
③	①&② Tolerance	± 0.051	± 0.038
④	Pad Misalignment	± 0.203	± 0.127
⑤	Pad Pitch Tolerance	± 0.051	± 0.038
⑥	Total Pad Pitch Tolerance	$\pm 0.8\%$ NLT ± 0.076	$\pm 0.5\%$ NLT ± 0.051
⑦	Pull-back (Recommendation)	(0.127)	

4.1.5 PIN GRID ARRAY (PGA)

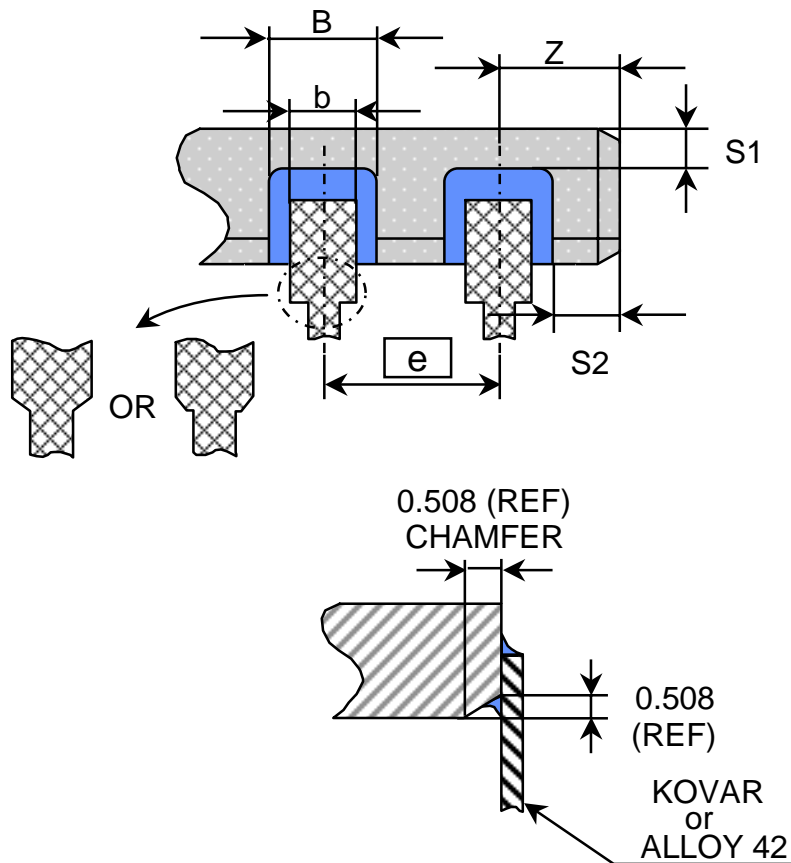


UNIT: mm

	Standard	Staggered	Surface Mount
e	2.54	1.796	1.27
Pin Grid			
ϕb	0.457	0.457	0.203
L	4.57	4.57	2.03
$\phi B1$	1.27	1.02	—
Z	2.03* 1.27	2.03* 1.27	1.27
$\phi B2$	1.65	1.27	0.86
Pin Material	Kovar Alloy42 Alloy194	Kovar Alloy42 Alloy194	Kovar

* NTK Recommendation

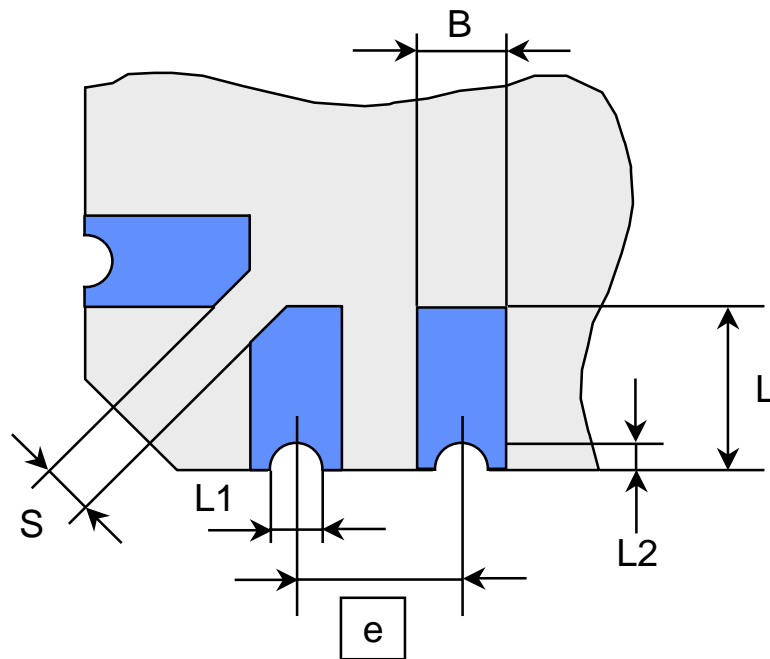
4.1.6 SIDE BRAZED PACKAGE



UNIT: mm

e	2.54	1.778	1.27
B	1.78 or 2.03	1.40	0.86 - 0.97
b	1.19 - 1.27	0.89	0.46
Z	1.27	TBD	TBD
S1	0.13 MIN	0.13 MIN	0.13 MIN
S2	0.13 MIN	0.13 MIN	0.13 MIN

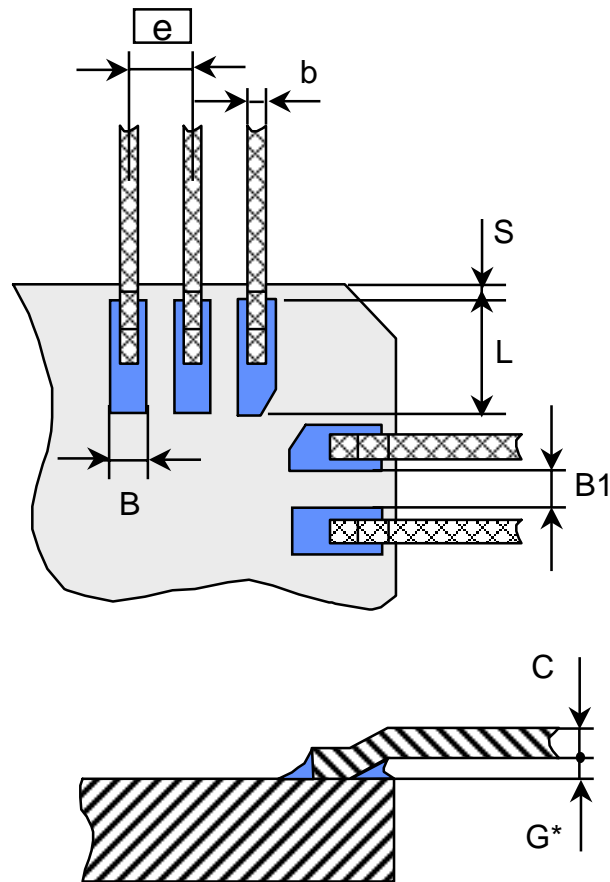
4.1.7 LEADLESS CHIP CARRIER (LCC)



UNIT:mm

e	1.27	1.016
L	1.27	1.016
B	0.635	0.381
L1	0.152 - 0.559	0.102 - 0.508
L2	0.076 - 0.381	0.076 - 0.381
S	0.381 MIN	0.381 MIN

4.1.8 FLAT LEAD PACKAGE

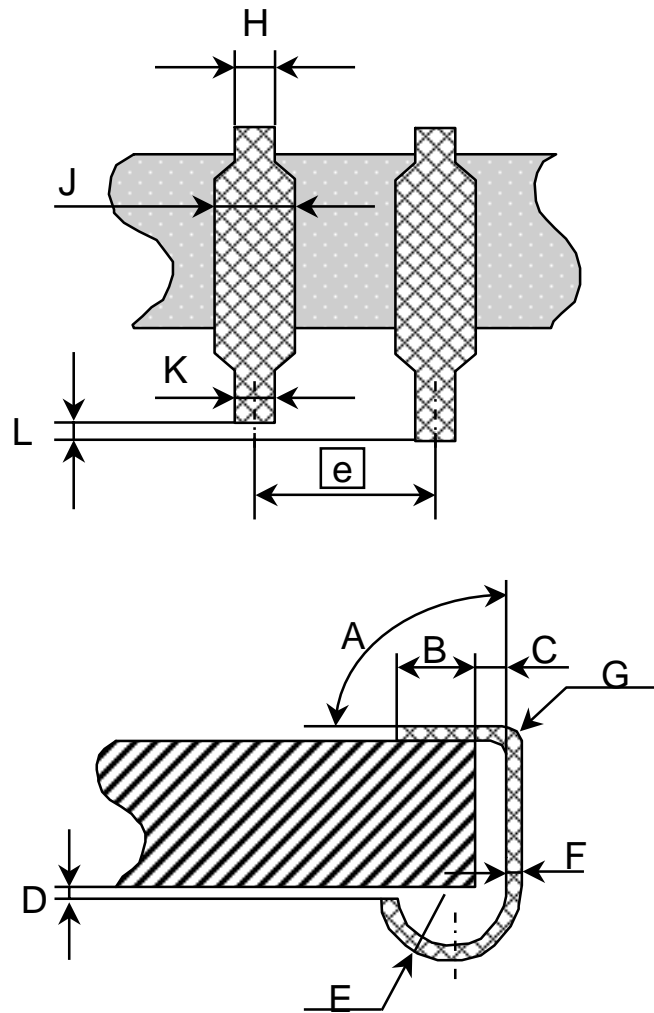


UNIT: mm

e	1.27	1.016	0.635	0.508	0.406	0.381
b	0.432	0.381	0.203	0.178	0.152	←
L	1.27	←	←	←	←	←
B	0.889	0.762	0.457	0.381	0.279	←
B1	0.381	0.254	0.178	0.127	←	0.102
C	0.127 or 0.152	←	0.152	←	←	←
G	0.229	←	←	←	←	←
S	0	←	0.127	←	←	←
LEAD MATERIAL	ALLOY 42 KOVAR	←	KOVAR	←	←	←

*DOG LEG LEAD FORMING

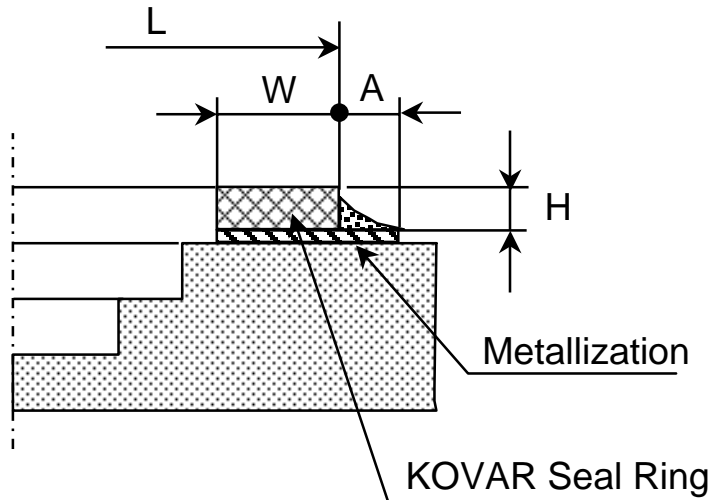
4.1.9 J LEAD PACKAGE



UNIT: mm

e	1.27
A	90 ±10 DEG.
B	1.02
C	0.305 REF
D	0.152 REF
E	0.762
F	0.178MIN - 0.229 MAX
G	R.381 REF
H	0.508
J	0.762
K	0.508
L	0.102 MAX

4.1.10 KOVAR SEAL RING



UNIT : mm

L	A
- 12.7	> 0.46
13.0 - 25.4	> 0.51
25.7 - 38.1	> 0.53
38.4 - 50.8	> 0.58
51.1 - 63.5	> 0.64
63.8 - 76.2	> 0.69
76.5 - 88.9	> 0.71
89.2 - 101.6	> 0.76

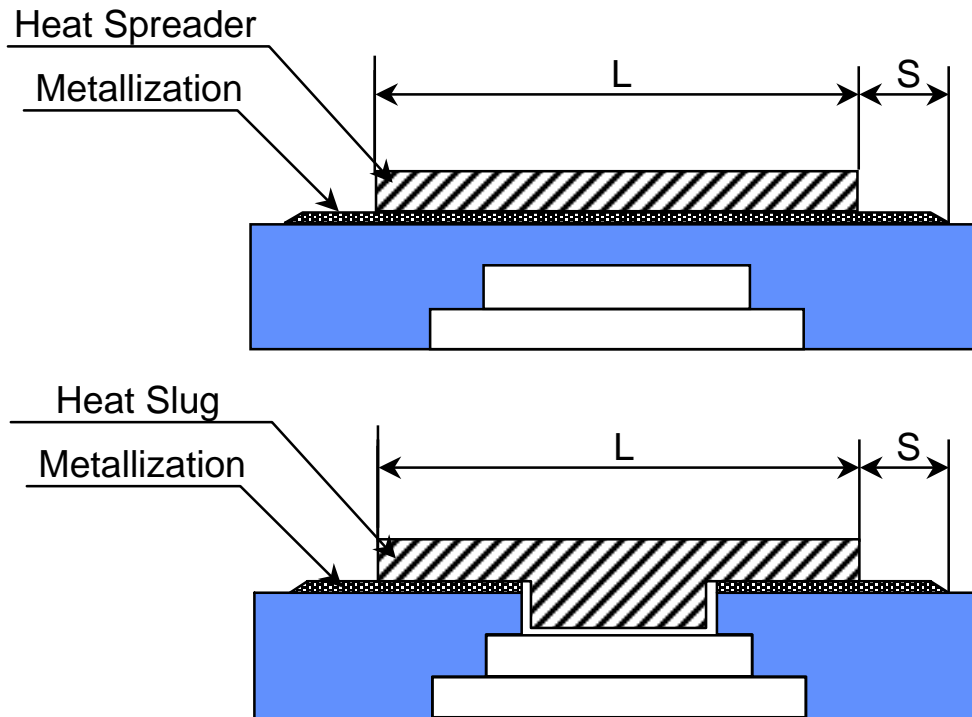
UNIT : mm

	Std. Thickness	Mfg. Method
H	0.254	Etching or Punching
	0.381	↑
	0.508*	Punching or Cutting
	0.635	↑
	0.762	↑
	1.016	↑

*NTK Recommendation

W	W > H
---	-------

4.1.11 HEAT SPREADER / HEAT SLUG



UNIT : mm

L	S (Recommendation)
< 30.5	≥ 1.27
≥ 30.5	≥ (1.27 + L x 1.0%)

4.1.12 PLATING

A. PLATING TYPE

< Electrolytic Plating >

UNIT : mm

Type	Ni	Au	Sn	Pb-Sn
#1	1.5 ~ 8.9	1.3 ~ 5.7	-----	-----
#2	↑	1.3 ~ 5.7*	-----	-----
#3	↑	-----	6.4 ~ 17.8	-----
#4	↑	-----	-----	6.4 ~ 17.8

* Except Outer Lead

<Electroless Plating>

UNIT : mm

Type	Ni	Au
#5	1.5 ~ 8.9	1.3 ~ 5.7
#6	↑	-----

- 1) Plating thickness depends on customer requirement.
- 2) Type #2 : Selective Au Plating
- 3) Type #3 and #4 : Multichip / Mother Board Package

B. Application

Application	Electrolytic				Electroless	
	#1 Ni + Au	#2 partial Au	#3 Ni + Sn	#4 Ni+Pb/Sn	#5 Ni + Au	#6 Ni
Die Attach						
(1) Au-Si Eutectic	○	○	----	----	○	----
(2) Epoxy	○	○	----	----	○	○
(3) Silver Glass	○ [1]	○ [1]	----	----	[2]	----
Wire Bonding						
(1) A1 Wire / U.S.	○	○	----	----	○	○
(2) Au Wire/ T.C.	○	○	----	----	○	----
(3) Au Wire / T.S.	○	○	----	----	○	----
Sealing						
(1) Au-Sn Preform	○	○	----	----	○	----
(2) Pb-Sn Solder	○	○	----	----	○	○
(3) Glass	○	----	----	----	[2]	----
(4) Epoxy	○	○	----	----	○	○
(5) Seam Welding [3]	○	○	----	----	○	○
Soldering	○	○	○	○	○	○ [4]

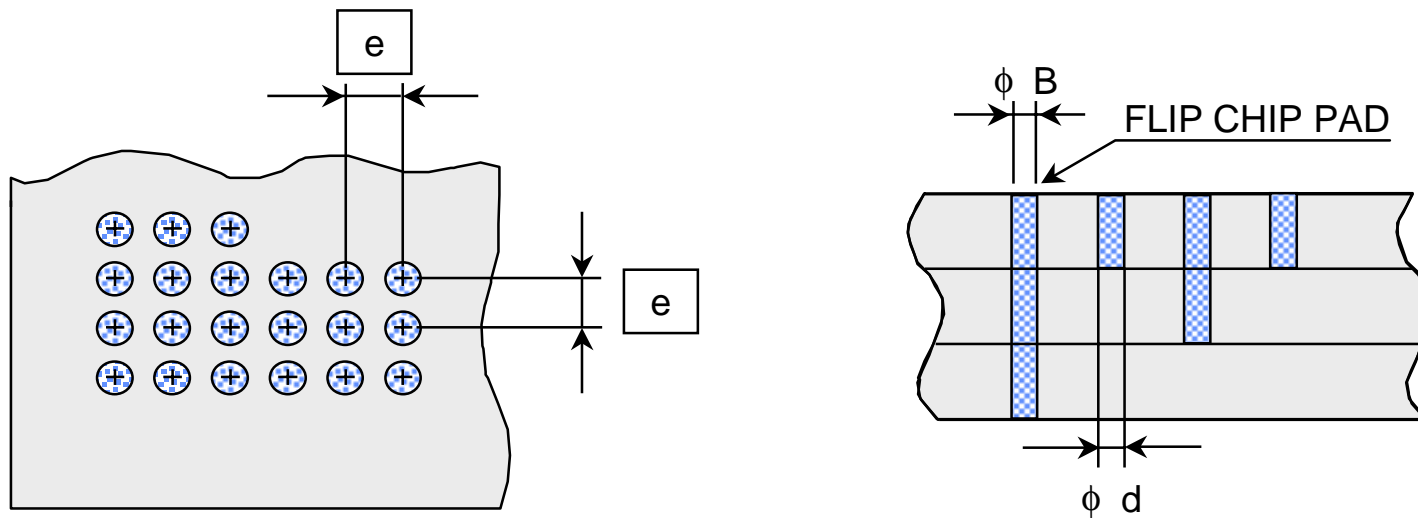
○ : Applicable
---- : Not Applicable

<Notes>

- [1] Need 2.5μmMIN. Au.
- [2] Please contact your local NTK sales engineer.
- [3] Needs brazed Kovar seal ring.
- [4] Need to remove oxide on Ni surface, if Au/Si or Ag-glass is used.

4.2 FLIP CHIP PACKAGE

4.2.1 STANDARD FLIP CHIP PAD DESIGN



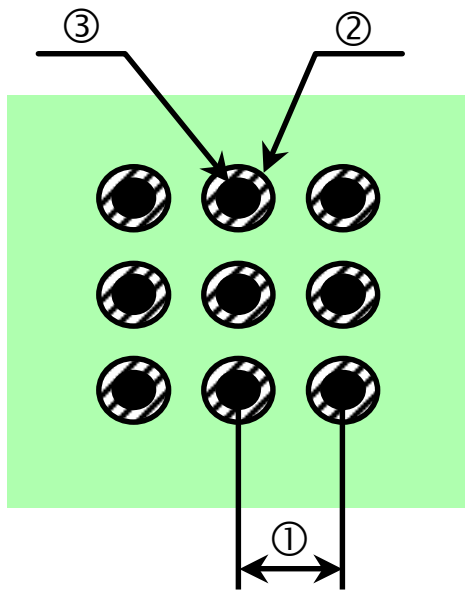
UNIT: mm

e	0.225 (Grid Array)
ϕB	0.102 (Via as F/C Pad)
ϕd	0.102

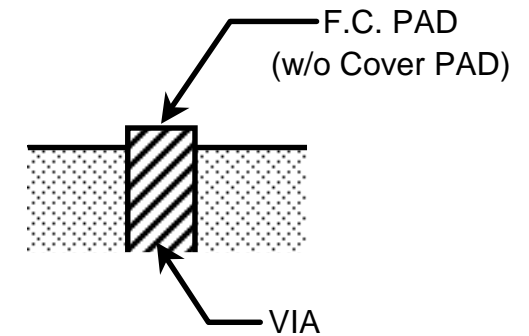
4.2.2 FLIP CHIP PAD DESIGN

(Std. design): No Cover Pad on Via
(Use Via as F/C Pad)

UNIT: μm



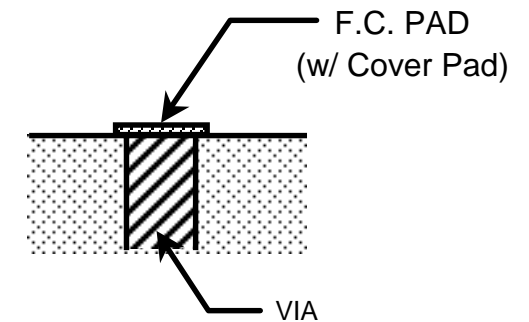
Item	Std.	Low Volume
① F/C Pad Pitch	≥ 225	≥ 180
② Via Diameter	100	≥ 70



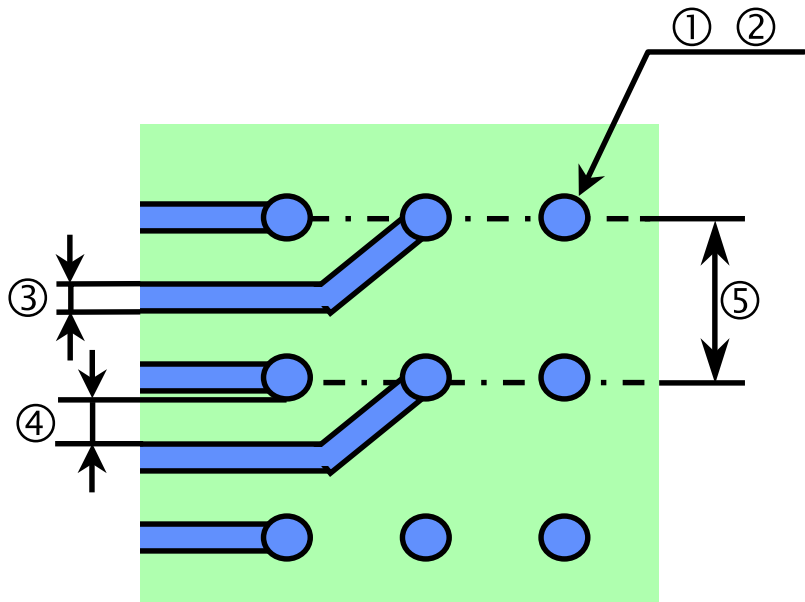
(Option): Cover Pad on Via

UNIT: μm

Item	Std.	Low Volume
① F/C Pad Pitch	≥ 225	≥ 200
② F/C Pad Dia.	≥ 125 (std. 140)	≥ 115
③ Via Diameter	100	≥ 70



4.2.3 INTERNAL SIGNAL UNDER FLIP CHIP PAD AREA

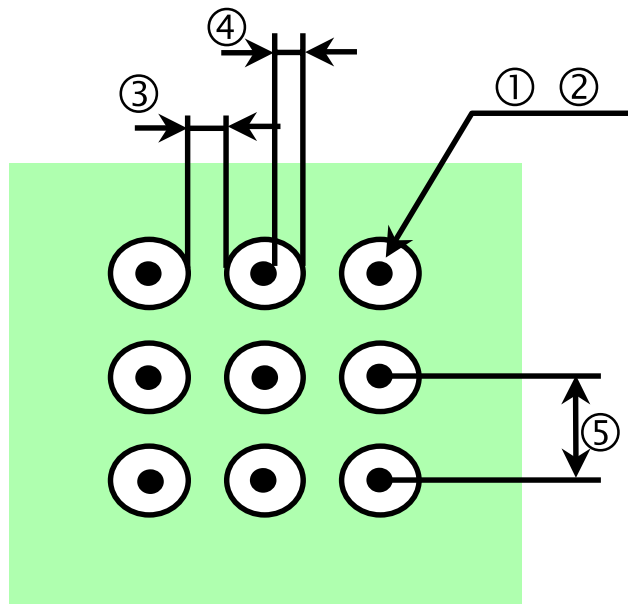


UNIT: μm

Item	Std.	Low Volume
① Via Diameter	100	≥ 70
② Cover Pad Diameter	100	≥ 70
③ Line Width	≥ 75	≥ 60
④ Metal Spacing	≥ 90	≥ 60
⑤ Minimum Via Pitch (1 Line between Vias)	≥ 355	≥ 250

4.2.4 INTERNAL PWR/GND PLANE UNDER FLIP CHIP PAD AREA

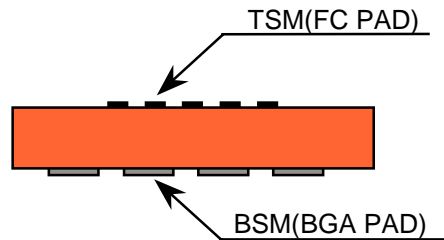
UNIT:μm



Item		Std.	Low Volume
①	Via Diameter	100	≥70
②	Cover Pad Diameter	100	≥70
③	Metal Width between Vias	≥50	≥30
④	Clearance	Layer Thk.≤102	≥130
		Layer Thk. >102	≥90
⑤	Via Pitch (w/ Metal Bridge between Vias)	Layer Thk.≤102	≥410
		Layer Thk.>102	≥330

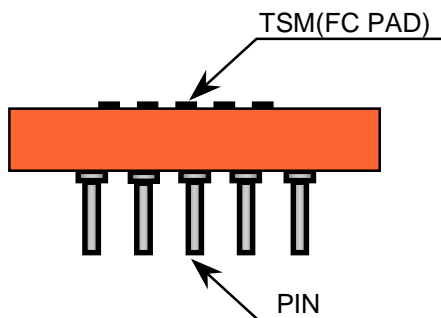
4.2.5 PLATING FOR FLIP CHIP PACKAGE

A. Flip Chip BGA



TSM	BSM
Electroless Ni (3.2μm Min.) +Electroless Au(0.03~0.10μm)	Electroless Ni (3.2μm Min.) +Electroless Au(0.03~0.10μm)

B. Flip Chip PGA



TSM	PIN (BSM)
Electroless Ni (3.2μm Min.) +Electroless Au(0.03~0.10μm)	Electrolytic Ni (2.0μm Min.) +Electrolytic Au(1.27μm Min.) (with Pin Through Plating)

5. SINGLE LAYER THIN FILM METALLIZED SUBSTRATE

5.1 OUTLINE

5.1.1 CERAMIC SUBSTRATE

UNIT: mm

Item		Pure Substrate	Co-fired Multilayer Substrate
Material		HA-995 BA-914 (HA-921) ALN	BA-914 (HA-921)
Size		≤ 102 SQ.	≤ 102 SQ.
Thickness		0.381 0.508 0.635	≤ 5.08 / TOTAL
Tolerance	O.D.	±0.203 (Laser Scribe) ± 0.051 (Dicing)	± 0.8%, NLT ± 0.127
	Thickness	± 10%, NLT ± 0.051 ± 0.051(Grinding)	± 10%, NLT ± 0.051 ± 0.051(Grinding)

5.1.2 THIN FILM CONSTITUTION (STD.)

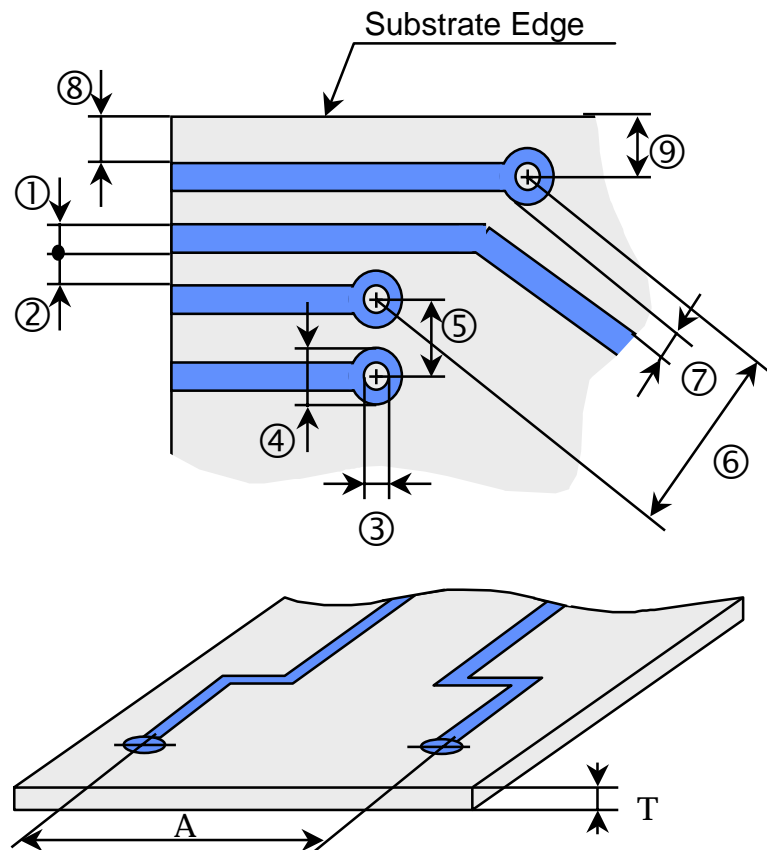
- 1) Ti-Pd-Au
- 2) Ti-Cu-Ni-Au
- 3) Ti-Mo-Cu-Ni-Au (for Ag/Cu Braze Type)

5.1.3 THIN FILM RESISTOR

- 1) Material : Tantalum Nitride (Ta₂N)
- 2) Sheet Resistance : 10 Ω / SQ ~ 50 Ω / SQ
- 3) Resistor Size : 0.102 SQ. MIN.

5.2 DESIGN RULE

5.2.1 THIN FILM METALLIZATION ON THE COFIRED CERAMIC SUBSTRATE



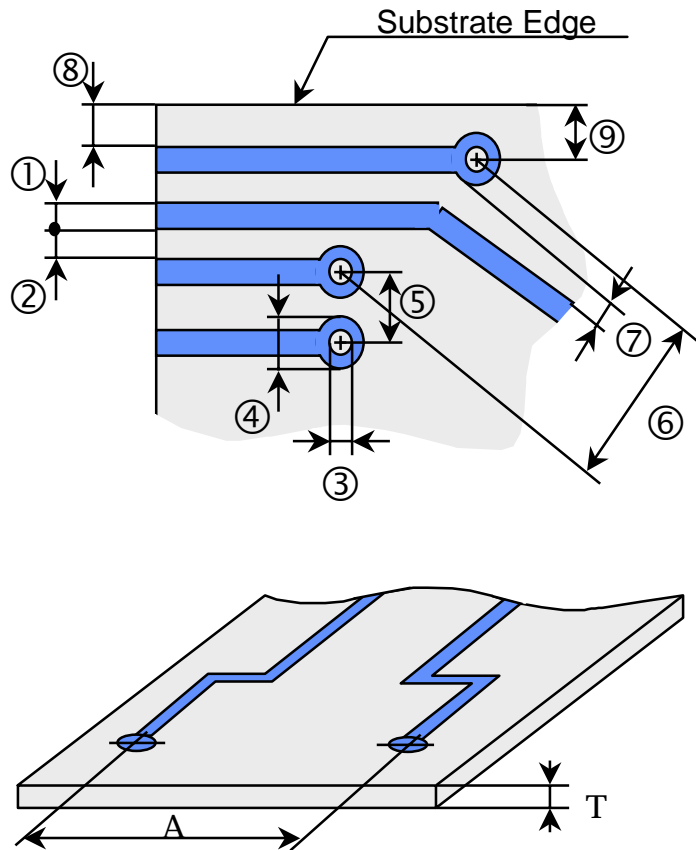
A : Maximum Via Pitch

UNIT: mm

LOCATION		LOW COST	STANDARD
①	Line Width	≥ 0.076	≥ 0.051
②	Line to Line Spacing	≥ 0.051	≥ 0.038
③	Via Diameter	≥ 0.152	≥ 0.102
④	Via Cover Pad Diameter	$\textcircled{3} + (\text{Ax}0.8\%) + 0.102$	$\textcircled{3} + (\text{Ax}0.8\%) + 0.102$
⑤	Via Pitch	≥ 0.635	≥ 0.254
⑥	Via Pitch (w/ 1 Line spacing)	$\textcircled{1} + \textcircled{4} + \textcircled{7} \times 2$	$\textcircled{1} + \textcircled{4} + \textcircled{7} \times 2$
⑦	Via Cover Pad to Line	≥ 0.041	≥ 0.030
⑧	Subst. Edge to Line Spacing	≥ 0.508	≥ 0.406
⑨	Subst. Edge to Via Spacing	≥ 0.635	≥ 0.381

5.2.2 THIN FILM METALLIZATION ON THE PURE CERAMIC SUBSTRATE

UNIT: mm



A : Maximum Via Pitch

LOCATION		LOW COST	STANDARD
①	Line Width	≥ 0.076	≥ 0.051
②	Line to Line Spacing	≥ 0.051	≥ 0.038
③	Via Hole Dia.	Punched Via	$\geq T, NLT \pm 0.152$
		Lasered Via	$\geq T, NLT \pm 0.254$
④	Via Hole Cover Pad Dia.	Punched Via	$\geq ③ + 0.008A + 0.102$
		Lasered Via	$\geq ③ + 0.102$
⑤	Via Hole Pitch	Punched Via	≥ 0.635
		Lasered Via	$\geq ③ + T + 0.102$
⑥	Via Hole Pitch (w/ 1 Line Spacing)	$① + ④ + ⑦ \times 2$	$① + ④ + ⑦ \times 2$
⑦	Via Cover Pad to Line Spacing	≥ 0.041	≥ 0.030
⑧	Subst. Edge to Line Spacing	≥ 0.508	≥ 0.406
⑨	Subst. Edge to Via Spacing	≥ 0.635	≥ 0.381



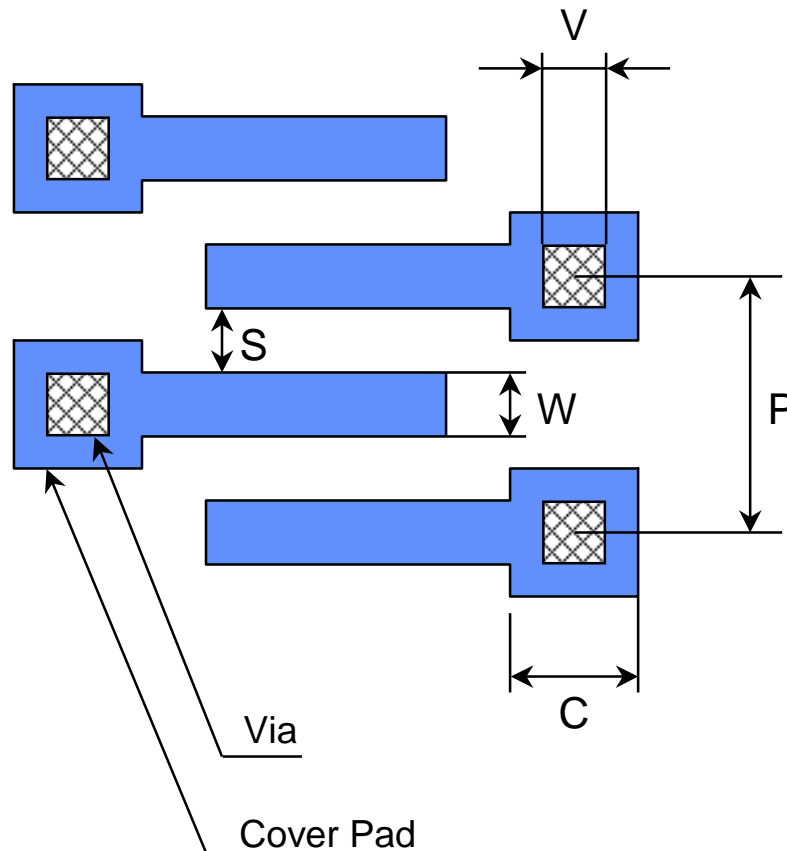
6. MULTILAYER THIN FILM SUBSTRATE (Cu-PI MULTILAYER)

6.1 OUTLINE

Item		Standard	Special
Substrate	Material Size	Alumina (HA-995,-96、BA-914) 100 μmSQ.MAX.	AlN
# of Layers	Conductor Dielectric	≤ 6 Layers ≤ 6 Layers	≤ 8 Layers ≤ 8 Layers
Conductor	Metallization - Top Surface - Internal Layer - Bottom Layer Thickness Line Width / Spacing	Cr-Ti-Cu-Ni-Au Cr-Ti-Cu-Ni-Pb/Sn Cr-Cu-Ni Ti-Cu-Ni (-Cr) ≤ 10 μm/Layer (by Request) 25μmMIN./50μmMIN.	Cr-Pd-Au、 Cr-Al 15μmMIN./30μmMIN.
Via	Size / Pitch	50μm/150μmMIN. (filled & stacked)	50μm/100μmMIN. (filled & staggered)
Dielectric	Material Thickness Dielectric Const./ Loss	Polyimide 10~25μm/Layer (by Request) 3.2/0.002 (@1MHz)	
Metal Parts Attach		Pin, Lead, and Ring Available	

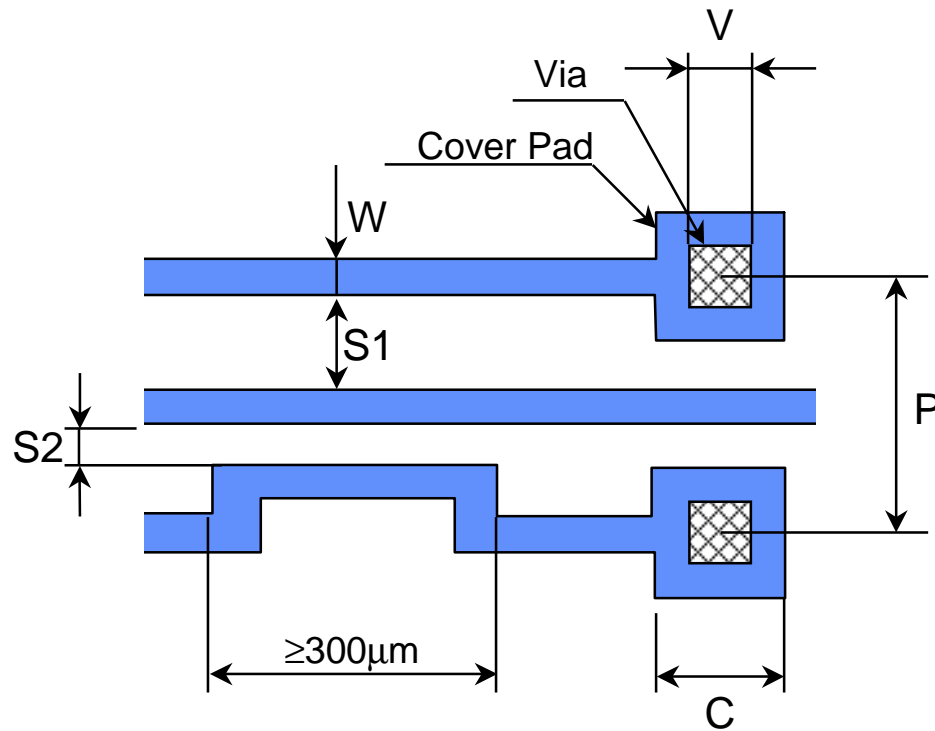
6.2 DESIGN RULE

6.2.1 TOP SURFACE METALLIZATION



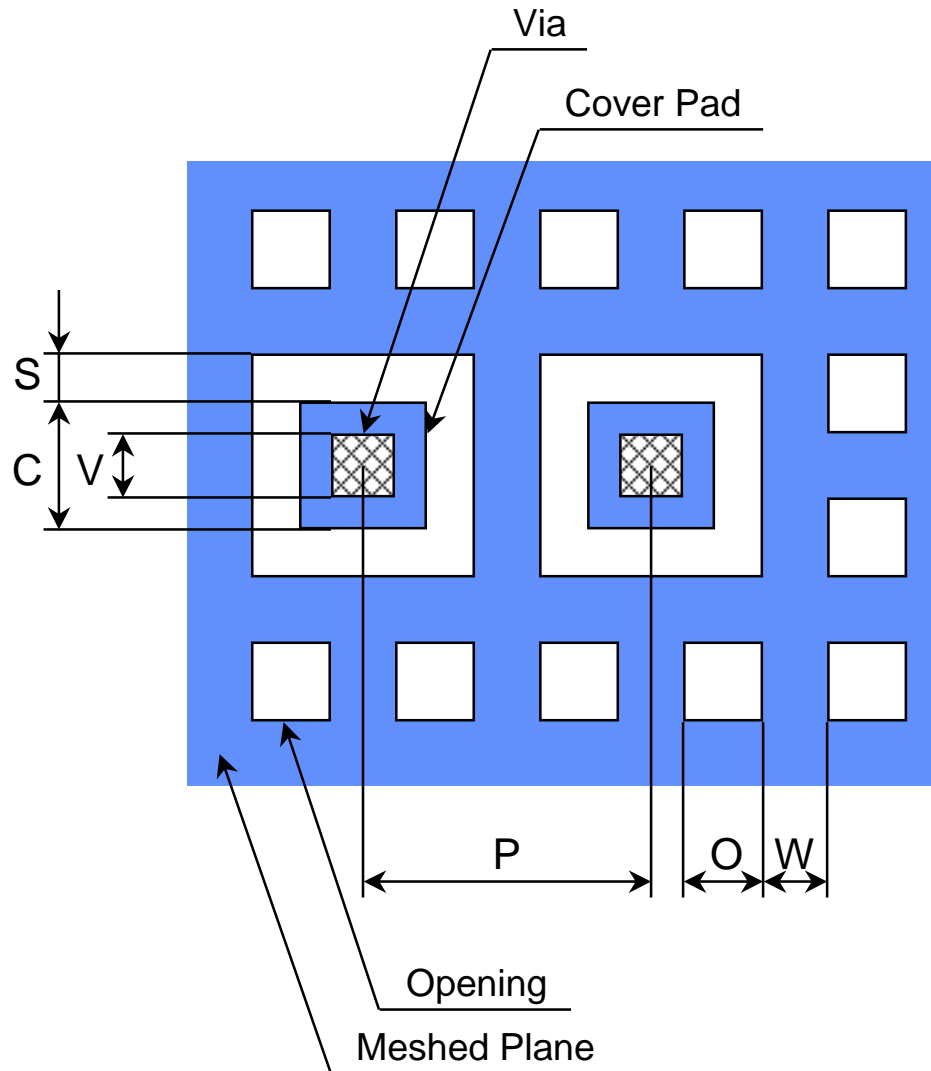
Location		Rule
W	Pad Width	$\geq 50 \mu\text{m}$
S	Pad Spacing	$\geq 50 \mu\text{m}$
V	Via Size (Filled Via)	$50 \mu\text{m}$
P	Via Pitch (Stacked Via)	$\geq 150 \mu\text{m}$
	(Staggered Via)	$\geq 100 \mu\text{m}$
C	Cover Pad Size	$\geq (V+20) \mu\text{m}$

6.2.2 INTERNAL TRACE



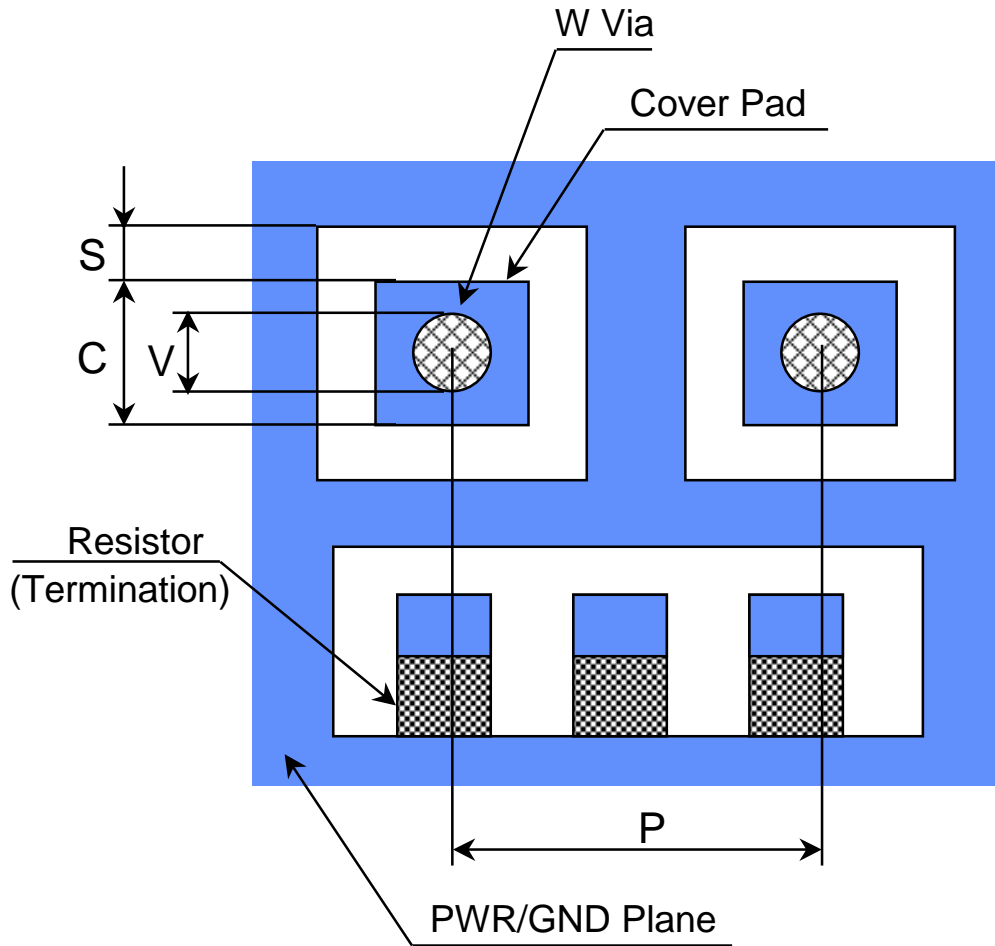
Location		Rule
W	Line Width	$\geq 25 \mu\text{m}$
S	Metal Spacing S1: Length < 300µm S2: Length $\geq 300\mu\text{m}$	$\geq 50 \mu\text{m}$ $\geq 30 \mu\text{m}$
V	Via Size (Filled Via)	$50 \mu\text{m}$
P	Via Pitch (Stacked Via) (Staggered Via)	$\geq 150 \mu\text{m}$ $\geq 100 \mu\text{m}$
C	Cover Pad Size	$\geq (V+20) \mu\text{m}$

6.2.3 INTERNAL PWR/GND PLANE



Location		Rule
W	Mesh Width	$\geq 50 \mu\text{m}$
O	Opening Size	$\geq W$
S	Clearance	$\geq 50 \mu\text{m}$
V	Via Size (Filled Via)	$50 \mu\text{m}$
P	Via Pitch (Stacked Via)	$\geq 150 \mu\text{m}$
	(Staggered Via)	$\geq 100 \mu\text{m}$
C	Cover Pad Size	$\geq (V+20) \mu\text{m}$

6.2.4 BOTTOM LAYER (PWR/GND PLANE ON THE CERAMIC SUBSTRATE)



	Location	Rule
S	Clearance	$\geq 100 \mu\text{m}$
V	Via Size	$\geq 100 \mu\text{m}$
C	Cover Pad Size D: Maximum Via Pitch T: Shrinkage Tolerance (STD: T=0.5%)	$\geq \{V+(D \times T)\}$
R	Resistor (Ta ₂ N)	$\geq 200 \mu\text{mSQ.}$